Zephyr Engineering, Inc

Specification, ZPCI.4096-02

Rev 1.0

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1. Introduction

The ZPCI.4096-02 is a 3U cPCI, 96-channel digital I/O board with rear-panel I/O on J2. Each of the 96 channels can be programmed as an input or as an output, independent of all other channels. Each channel can be programmed to cause an interrupt either on a rising (low-to-high) or falling (high-to-low) transition or both rising and falling transitions. The interrupt from each channel can be individually masked.

2. Functional Blocks

3. Register Descriptions

The ZPCI.4096 PCI FPGA implements 13 internal registers. These registers are described below. The following table shows the memory map for the ZPCI-4096-02:

PCI Offset	Register Name	# bits	Register Description
00	DR0	32	Ch 31-0 data in/out register
04	DR1	32	Ch 63-32 data in/out register
08	DR2	32	Ch 95-64 data in/out register
0C	(reserved)	32	
10	OER0	32	Ch 31-0 output enable register
14	OER1	32	Ch 63-32 output enable register
18	OER2	32	Ch 95-64 output enable register
1C	(reserved)	32	
20	ISR0	32	Ch 31-0 interrupt status register
24	ISR1	32	Ch 63-32 interrupt status register
28	ISR2	32	Ch 95-64 interrupt status register
2C	(reserved)	32	
30	IER0	32	Ch 31-0 interrupt enable register
34	IER1	32	Ch 63-32 interrupt enable register
38	IER2	32	Ch 95-64 interrupt enable register
3C	(reserved)	32	
40	RER0	32	Ch 31-0 rising edge enable register
44	RER1	32	Ch 63-32 rising edge enable register
48	RER2	32	Ch 95-64 rising edge enable register
4C	(reserved)	32	
50	FER0	32	Ch 31-0 falling edge enable register
54	FER1	32	Ch 63-32 falling edge enable register
58	FER2	32	Ch 95-64 falling edge enable register
5C	(reserved)	32	
60	CDR0	32	Ch 31-0 change detect register
64	CDR1	32	Ch 63-32 change detect register
68	CDR2	32	Ch 95-64 change detect register
6C	(reserved)	32	
70	CSR	32	control and status register
74	WDR	32	watchdog control and status register
78	WCLR	32	watchdog clear register
7C	(reserved)	32	

Note that the ZPCI.4096-02 requests 4KB of memory space on the PCI bus because that is the minimum BAR size. However, only the lower seven (7) address bits are considered for on-board address decoding. Thus, this memory maps repeats at PCI offsets of 080h, 100h, 180h, and so forth up to F80h.

3.1 Data In/Out Registers (DR0 – DR2)

On reset, DR0 – DR2 output registers contain 0. Since all bits are reset to inputs on power-up, the value read will reflect a state as determined by the external connections to the DIO_n pins. All pins are externally pulled up to 3.3V with a 22K ohm resistor. Unconnected pins will therefore read back as logic "1".

DR2:

bit 31	30	29	28	27	26	25	bit 24
0	0	0	0	0	0	0	0
DIO_95	DIO_94	DIO_93	DIO_92	DIO_91	DIO_90	DIO_89	DIO_88

bit 23	22	21	20	19	18	17	bit 16
0	0	0	0	0	0	0	0
DIO_87	DIO_86	DIO_85	DIO_84	DIO_83	DIO_82	DIO_81	DIO_80

bit 15	14	13	12	11	10	9	bit 8
0	0	0	0	0	0	0	0
DIO_79	DIO_78	DIO_77	DIO_76	DIO_75	DIO_74	DIO_73	DIO_72

bit 7	6	5	4	3	2	1	bit 0
0	0	0	0	0	0	0	0
DIO_71	DIO_70	DIO_69	DIO_68	DIO_67	DIO_66	DIO_65	DIO_64

DIO_95 – DIO_64: Data In/Out (R/W)

On read, this register reflects the actual state of the DIO_n pin on the FPGA.
On write, if OE_n is set in OER2, the write value will be driven onto the pin.
If OE_n is not set in OER2, writes are stored but not driven onto the pin.
1 = DIO_n pin is high (read); drive DIO_n high if enabled in OER2 (write)
0 = DIO_n pin is low (read); drive DIO_n low if enabled in OER2 (write)

DR1:

bit 31	30	29	28	27	26	25	bit 24
0	0	0	0	0	0	0	0
DIO_63	DIO_62	DIO_61	DIO_60	DIO_59	DIO_58	DIO_57	DIO_56

bit 23	22	21	20	19	18	17	bit 16
0	0	0	0	0	0	0	0
DIO_55	DIO_54	DIO_53	DIO_52	DIO_51	DIO_50	DIO_49	DIO_48

bit 15	14	13	12	11	10	9	bit 8
0	0	0	0	0	0	0	0
DIO_47	DIO_46	DIO_45	DIO_44	DIO_43	DIO_42	DIO_41	DIO_40

bit 7	6	5	4	3	2	1	bit 0
0	0	0	0	0	0	0	0
DIO_39	DIO_38	DIO_37	DIO_36	DIO_35	DIO_34	DIO_33	DIO_32

DIO_63 – DIO_32: Data In/Out (R/W)

On read, this register reflects the actual state of the DIO_n pin on the FPGA.
On write, if OE_n is set in OER1, the write value will be driven onto the pin.
If OE_n is not set in OER1, writes are stored but not driven onto the pin.
1 = DIO_n pin is high (read); drive DIO_n high if enabled in OER1 (write)
0 = DIO_n pin is low (read); drive DIO_n low if enabled in OER1 (write)

DR0:

bit 31	30	29	28	27	26	25	bit 24
0	0	0	0	0	0	0	0
DIO_31	DIO_30	DIO_29	DIO_28	DIO_27	DIO_26	DIO_25	DIO_24

bit 23	22	21	20	19	18	17	bit 16
0	0	0	0	0	0	0	0
DIO_23	DIO_22	DIO_21	DIO_20	DIO_19	DIO_18	DIO_17	DIO_16

bit 15	14	13	12	11	10	9	bit 8
0	0	0	0	0	0	0	0
DIO_15	DIO_14	DIO_13	DIO_12	DIO_11	DIO_10	DIO_9	DIO_8

bit 7	6	5	4	3	2	1	bit 0
0	0	0	0	0	0	0	0
DIO_7	DIO_6	DIO_5	DIO_4	DIO_3	DIO_2	DIO_1	DIO_0

DIO_31 – DIO_0: Data In/Out (R/W)

On read, this register reflects the actual state of the DIO_n pin on the FPGA.
On write, if OE_n is set in OER0, the write value will be driven onto the pin.
If OE_n is not set in OER0, writes are stored but not driven onto the pin.
1 = DIO_n pin is high (read); drive DIO_n high if enabled in OER0 (write)
0 = DIO_n pin is low (read); drive DIO_n low if enabled in OER0 (write)

3.2 Output Enable Registers (OER0 – OER2)

The default value of each OER_n register bit on reset is shown just above the bit assignments.

OER2:

bit 31	30	29	28	27	26	25	bit 24
0	0	0	0	0	0	0	0
OE_95	OE_94	OE_93	OE_92	OE_91	OE_90	OE_89	OE_88

bit 23	22	21	20	19	18	17	bit 16
0	0	0	0	0	0	0	0
OE_87	OE_86	OE_85	OE_84	OE_83	OE_82	OE_81	OE_80

bit 15	14	13	12	11	10	9	bit 8
0	0	0	0	0	0	0	0
OE_79	OE_78	OE_77	OE_76	OE_75	OE_74	OE_73	OE_72

bit 7	6	5	4	3	2	1	bit 0
0	0	0	0	0	0	0	0
OE_71	OE_70	OE_69	OE_68	OE_67	OE_66	OE_65	OE_64

OE_95 – OE_64: Output Enable (R/W)
1 = DIO_n pin output is enabled
0 = DIO_n pin is input only; all writes to DIO_n in DR2 are stored but not driven.

OER1:

bit 31	30	29	28	27	26	25	bit 24
0	0	0	0	0	0	0	0
OE_63	OE_62	OE_61	OE_60	OE_59	OE_58	OE_57	OE_56

bit 23	22	21	20	19	18	17	bit 16
0	0	0	0	0	0	0	0
OE_55	OE_54	OE_53	OE_52	OE_51	OE_50	OE_49	OE_48

bit 15	14	13	12	11	10	9	bit 8
0	0	0	0	0	0	0	0
OE_47	OE_46	OE_45	OE_44	OE_43	OE_42	OE_41	OE_40

bit 7	6	5	4	3	2	1	bit 0
0	0	0	0	0	0	0	0
OE_39	OE_38	OE_37	OE_36	OE_35	OE_34	OE_33	OE_32

OE_63 – OE_32: Output Enable (R/W)
1 = DIO_n pin output is enabled
0 = DIO_n pin is input only; all writes to DIO_n in DR1 are stored but not driven

OER0:

bit 31	30	29	28	27	26	25	bit 24
0	0	0	0	0	0	0	0
OE_31	OE_30	OE_29	OE_28	OE_27	OE_26	OE_25	OE_24

bit 23	22	21	20	19	18	17	bit 16
0	0	0	0	0	0	0	0
OE_23	OE_22	OE_21	OE_20	OE_19	OE_18	OE_17	OE_16

bit 15	14	13	12	11	10	9	bit 8
0	0	0	0	0	0	0	0
OE_15	OE_14	OE_13	OE_12	OE_11	OE_10	OE_9	OE_8

bit 7	6	5	4	3	2	1	bit 0
0	0	0	0	0	0	0	0
OE_7	OE_6	OE_5	OE_4	OE_3	OE_2	OE_1	OE_0

OE_31 – OE_0: Output Enable (R/W)
1 = DIO_n pin output is enabled
0 = DIO_n pin is input only; all writes to DIO_n in DR0 are stored but not driven

3.3 Interrupt Status Registers (ISR0 – ISR2)

The default value of each ISR_n register bit on reset is shown just above the bit assignments.

ISR2:

bit 31	30	29	28	27	26	25	bit 24
0	0	0	0	0	0	0	0
IS_95	IS_94	IS_93	IS_92	IS_91	IS_90	IS_89	IS_88

bit 23	22	21	20	19	18	17	bit 16
0	0	0	0	0	0	0	0
IS_87	IS_86	IS_85	IS_84	IS_83	IS_82	IS_81	IS_80

bit 15	14	13	12	11	10	9	bit 8
0	0	0	0	0	0	0	0
IS_79	IS_78	IS_77	IS_76	IS_75	IS_74	IS_73	IS_72

bit 7	6	5	4	3	2	1	bit 0
0	0	0	0	0	0	0	0
IS_71	IS_70	IS_69	IS_68	IS_67	IS_66	IS_65	IS_64

IS_95 – IS_64: Interrupt Status (R/W)

On read:
1 = IE_n (interrupt enabled) and CD_n (edge detected) are both set
0 = either IE_n is clear (interrupt masked) or CD_n is clear (no edge detected)

On write:
1 = clear both the IS_n and CD_n bits to 0
0 = do nothing

ISR1:

bit 31	30	29	28	27	26	25	bit 24
0	0	0	0	0	0	0	0
IS_63	IS_62	IS_61	IS_60	IS_59	IS_58	IS_57	IS_56

bit 23	22	21	20	19	18	17	bit 16
0	0	0	0	0	0	0	0
IS_55	IS_54	IS_53	IS_52	IS_51	IS_50	IS_49	IS_48

bit 15	14	13	12	11	10	9	bit 8
0	0	0	0	0	0	0	0
IS_47	IS_46	IS_45	IS_44	IS_43	IS_42	IS_41	IS_40

bit 7	6	5	4	3	2	1	bit 0
0	0	0	0	0	0	0	0
IS_39	IS_38	IS_37	IS_36	IS_35	IS_34	IS_33	IS_32

IS_63 – IS_32: Interrupt Request (R/W)

On read:
1 = IE_n (interrupt enabled) and CD_n (edge detected) are both set
0 = either IE_n is clear (interrupt masked) or CD_n is clear (no edge detected)

On write:
1 = clear both the IS_n and CD_n bits to 0
0 = do nothing

ISR0:

bit 31	30	29	28	27	26	25	bit 24
0	0	0	0	0	0	0	0
IS_31	IS_30	IS_29	IS_28	IS_27	IS_26	IS_25	IS_24

bit 23	22	21	20	19	18	17	bit 16
0	0	0	0	0	0	0	0
IS_23	IS_22	IS_21	IS_20	IS_19	IS_18	IS_17	IS_16

bit 15	14	13	12	11	10	9	bit 8
0	0	0	0	0	0	0	0
IS_15	IS_14	IS_13	IS_12	IS_11	IS_10	IS_9	IS_8

bit 7	6	5	4	3	2	1	bit 0
0	0	0	0	0	0	0	0
IS_7	IS_6	IS_5	IS_4	IS_3	IS_2	IS_1	IS_0

IS_31 – IS_0: Interrupt Request (R/W)

On read:
1 = IE_n (interrupt enabled) and CD_n (edge detected) are both set
0 = either IE_n is clear (interrupt masked) or CD_n is clear (no edge detected)

On write:
1 = clear both the IS_n and CD_n bits to 0
0 = do nothing

3.4 Interrupt Enable Registers (IER0 – IER2)

The default value of each IER_n register bit on reset is shown just above the bit assignments.

IER2:

bit 31	30	29	28	27	26	25	bit 24
0	0	0	0	0	0	0	0
IE_95	IE_94	IE_93	IE_92	IE_91	IE_90	IE_89	IE_88

bit 23	22	21	20	19	18	17	bit 16
0	0	0	0	0	0	0	0
IE_87	IE_86	IE_85	IE_84	IE_83	IE_82	IE_81	IE_80

bit 15	14	13	12	11	10	9	bit 8
0	0	0	0	0	0	0	0
IE_79	IE_78	IE_77	IE_76	IE_75	IE_74	IE_73	IE_72

bit 7	6	5	4	3	2	1	bit 0
0	0	0	0	0	0	0	0
IE_71	IE_70	IE_69	IE_68	IE_67	IE_66	IE_65	IE_64

IE_95 – IE_64: Interrupt Enable (R/W)

1 = allow CD_n assertion to cause assertion of IS_n (and INTA# if CDIEN is set)
0 = CD_n assertion does not cause assertion of IS_n

IER1:

bit 31	30	29	28	27	26	25	bit 24
0	0	0	0	0	0	0	0
IE_63	IE_62	IE_61	IE_60	IE_59	IE_58	IE_57	IE_56

bit 23	22	21	20	19	18	17	bit 16
0	0	0	0	0	0	0	0
IE_55	IE_54	IE_53	IE_52	IE_51	IE_50	IE_49	IE_48

bit 15	14	13	12	11	10	9	bit 8
0	0	0	0	0	0	0	0
IE_47	IE_46	IE_45	IE_44	IE_43	IE_42	IE_41	IE_40

bit 7	6	5	4	3	2	1	bit 0
0	0	0	0	0	0	0	0
IE_39	IE_38	IE_37	IE_36	IE_35	IE_34	IE_33	IE_32

IE_63 – IE_32: Interrupt Enable (R/W)
1 = allow CD_n assertion to cause assertion of IS_n (and INTA# if CDIEN is set)
0 = CD_n assertion does not cause assertion of IS_n

IER0:

bit 31	30	29	28	27	26	25	bit 24
0	0	0	0	0	0	0	0
IE_31	IE_30	IE_29	IE_28	IE_27	IE_26	IE_25	IE_24

bit 23	22	21	20	19	18	17	bit 16
0	0	0	0	0	0	0	0
IE_23	IE_22	IE_21	IE_20	IE_19	IE_18	IE_17	IE_16

bit 15	14	13	12	11	10	9	bit 8
0	0	0	0	0	0	0	0
IE_15	IE_14	IE_13	IE_12	IE_11	IE_10	IE_9	IE_8

bit 7	6	5	4	3	2	1	bit 0
0	0	0	0	0	0	0	0
IE_7	IE_6	IE_5	IE_4	IE_3	IE_2	IE_1	IE_0

IE_31 – IE_0: Interrupt Enable (R/W)
1 = allow CD_n assertion to cause assertion of IS_n (and INTA# if CDIEN is set)
0 = CD_n assertion does not cause assertion of IS_n

3.5 Rising Edge Enable Registers (RER0 – RER2)

The default value of each RER_n register bit on reset is shown just above the bit assignments.

RER2:

bit 31	30	29	28	27	26	25	bit 24
0	0	0	0	0	0	0	0
RE_95	RE_94	RE_93	RE_92	RE_91	RE_90	RE_89	RE_88

bit 23	22	21	20	19	18	17	bit 16
0	0	0	0	0	0	0	0
RE_87	RE_86	RE_85	RE_84	RE_83	RE_82	RE_81	RE_80

bit 15	14	13	12	11	10	9	bit 8
0	0	0	0	0	0	0	0
RE_79	RE_78	RE_77	RE_76	RE_75	RE_74	RE_73	RE_72

bit 7	6	5	4	3	2	1	bit 0
0	0	0	0	0	0	0	0
RE_71	RE_70	RE_69	RE_68	RE_67	RE_66	RE_65	RE_64

RE_95 – RE_64: Rising Edge Enable (R/W)
1 = set CD_n whenever a rising (low-to-high) transition is detected on DIO_n
0 = ignore rising (low-to-high) transitions on DIO_n

RER1:

bit 31	30	29	28	27	26	25	bit 24
0	0	0	0	0	0	0	0
RE_63	RE_62	RE_61	RE_60	RE_59	RE_58	RE_57	RE_56

bit 23	22	21	20	19	18	17	bit 16
0	0	0	0	0	0	0	0
RE_55	RE_54	RE_53	RE_52	RE_51	RE_50	RE_49	RE_48

bit 15	14	13	12	11	10	9	bit 8
0	0	0	0	0	0	0	0
RE_47	RE_46	RE_45	RE_44	RE_43	RE_42	RE_41	RE_40

bit 7	6	5	4	3	2	1	bit 0
0	0	0	0	0	0	0	0
RE_39	RE_38	RE_37	RE_36	RE_35	RE_34	RE_33	RE_32

RE_63 – RE_32: Rising Edge Enable (R/W)
1 = set CD_n whenever a rising (low-to-high) transition is detected on DIO_n
0 = ignore rising (low-to-high) transitions on DIO_n

RER0:

bit 31	30	29	28	27	26	25	bit 24
0	0	0	0	0	0	0	0
RE_31	RE_30	RE_29	RE_28	RE_27	RE_26	RE_25	RE_24

bit 23	22	21	20	19	18	17	bit 16
0	0	0	0	0	0	0	0
RE_23	RE_22	RE_21	RE_20	RE_19	RE_18	RE_17	RE_16

bit 15	14	13	12	11	10	9	bit 8
0	0	0	0	0	0	0	0
RE_15	RE_14	RE_13	RE_12	RE_11	RE_10	RE_9	RE_8

bit 7	6	5	4	3	2	1	bit 0
0	0	0	0	0	0	0	0
RE_7	RE_6	RE_5	RE_4	RE_3	RE_2	RE_1	RE_0

RE_31 – RE_0: Rising Edge Enable (R/W)
1 = set CD_n whenever a rising (low-to-high) transition is detected on DIO_n
0 = ignore rising (low-to-high) transitions on DIO_n

3.6 Falling Edge Enable Registers (FER0 – FER2)

The default value of each FER_n register bit on reset is shown just above the bit assignments.

FER2:

bit 31	30	29	28	27	26	25	bit 24
0	0	0	0	0	0	0	0
FE_95	FE_94	FE_93	FE_92	FE_91	FE_90	FE_89	FE_88

bit 23	22	21	20	19	18	17	bit 16
0	0	0	0	0	0	0	0
FE_87	FE_86	FE_85	FE_84	FE_83	FE_82	FE_81	FE_80

bit 15	14	13	12	11	10	9	bit 8
0	0	0	0	0	0	0	0
FE_79	FE_78	FE_77	FE_76	FE_75	FE_74	FE_73	FE_72

bit 7	6	5	4	3	2	1	bit 0
0	0	0	0	0	0	0	0
FE_71	FE_70	FE_69	FE_68	FE_67	FE_66	FE_65	FE_64

FE_95 – FE_64: Falling Edge Enable (R/W)
1 = set CD_n whenever a falling (high-to-low) transition is detected on DIO_n
0 = ignore falling (high-to-low) transitions on DIO_n

FER1:

bit 31	30	29	28	27	26	25	bit 24
0	0	0	0	0	0	0	0
FE_63	FE_62	FE_61	FE_60	FE_59	FE_58	FE_57	FE_56

bit 23	22	21	20	19	18	17	bit 16
0	0	0	0	0	0	0	0
FE_55	FE_54	FE_53	FE_52	FE_51	FE_50	FE_49	FE_48

bit 15	14	13	12	11	10	9	bit 8
0	0	0	0	0	0	0	0
FE_47	FE_46	FE_45	FE_44	FE_43	FE_42	FE_41	FE_40

bit 7	6	5	4	3	2	1	bit 0
0	0	0	0	0	0	0	0
FE_39	FE_38	FE_37	FE_36	FE_35	FE_34	FE_33	FE_32

FE_63 – FE_32: Falling Edge Enable (R/W)
1 = set CD_n whenever a falling (high-to-low) transition is detected on DIO_n
0 = ignore falling (high-to-low) transitions on DIO_n

FER0:

bit 31	30	29	28	27	26	25	bit 24
0	0	0	0	0	0	0	0
FE_31	FE_30	FE_29	FE_28	FE_27	FE_26	FE_25	FE_24

bit 23	22	21	20	19	18	17	bit 16
0	0	0	0	0	0	0	0
FE_23	FE_22	FE_21	FE_20	FE_19	FE_18	FE_17	FE_16

bit 15	14	13	12	11	10	9	bit 8
0	0	0	0	0	0	0	0
FE_15	FE_14	FE_13	FE_12	FE_11	FE_10	FE_9	FE_8

bit 7	6	5	4	3	2	1	bit 0
0	0	0	0	0	0	0	0
FE_7	FE_6	FE_5	FE_4	FE_3	FE_2	FE_1	FE_0

FE_31 – FE_0: Falling Edge Enable (R/W)
1 = set CD_n whenever a falling (high-to-low) transition is detected on DIO_n
0 = ignore falling (high-to-low) transitions on DIO_n

3.7 Change Detect Registers (CDR0 – CDR2)

The default value of each CDR_n register bit on reset is shown just above the bit assignments.

CDR2:

bit 31	30	29	28	27	26	25	bit 24
0	0	0	0	0	0	0	0
CD_95	CD_94	CD_93	CD_92	CD_91	CD_90	CD_89	CD_88

bit 23	22	21	20	19	18	17	bit 16
0	0	0	0	0	0	0	0
CD_87	CD_86	CD_85	CD_84	CD_83	CD_82	CD_81	CD_80

bit 15	14	13	12	11	10	9	bit 8
0	0	0	0	0	0	0	0
CD_79	CD_78	CD_77	CD_76	CD_75	CD_74	CD_73	CD_72

bit 7	6	5	4	3	2	1	bit 0
0	0	0	0	0	0	0	0
CD_71	CD_70	CD_69	CD_68	CD_67	CD_66	CD_65	CD_64

CD_95 – CD_64: Change Detect (R/W)

On read:
1 = specified change has been detected on DIO_n since last clear of CD_n
0 = specified change has not been detected on DIO_n since last clear of CD_n

On write:
1 = set the CD_n bit to 1
0 = do nothing

CDR1:

bit 31	30	29	28	27	26	25	bit 24
0	0	0	0	0	0	0	0
CD_63	CD_62	CD_61	CD_60	CD_59	CD_58	CD_57	CD_56

bit 23	22	21	20	19	18	17	bit 16
0	0	0	0	0	0	0	0
CD_55	CD_54	CD_53	CD_52	CD_51	CD_50	CD_49	CD_48

bit 15	14	13	12	11	10	9	bit 8
0	0	0	0	0	0	0	0
CD_47	CD_46	CD_45	CD_44	CD_43	CD_42	CD_41	CD_40

bit 7	6	5	4	3	2	1	bit 0
0	0	0	0	0	0	0	0
CD_39	CD_38	CD_37	CD_36	CD_35	CD_34	CD_33	CD_32

CD_63 – CD_32: Change Detect (R/W)

On read:
1 = specified change has been detected on DIO_n since last clear of CD_n
0 = specified change has not been detected on DIO_n since last clear of CD_n

On write:
1 = set the CD_n bit to 1
0 = do nothing

CDR0:

bit 31	30	29	28	27	26	25	bit 24
0	0	0	0	0	0	0	0
CD_31	CD_30	CD_29	CD_28	CD_27	CD_26	CD_25	CD_24

bit 23	22	21	20	19	18	17	bit 16
0	0	0	0	0	0	0	0
CD_23	CD_22	CD_21	CD_20	CD_19	CD_18	CD_17	CD_16

bit 15	14	13	12	11	10	9	bit 8
0	0	0	0	0	0	0	0
CD_15	CD_14	CD_13	CD_12	CD_11	CD_10	CD_9	CD_8

bit 7	6	5	4	3	2	1	bit 0
0	0	0	0	0	0	0	0
CD_7	CD_6	CD_5	CD_4	CD_3	CD_2	CD_1	CD_0

CD_31 – CD_0: Change Detect (R/W)

On read:
1 = specified change has been detected on DIO_n since last clear of CD_n
0 = specified change has not been detected on DIO_n since last clear of CD_n

On write:
1 = set the CD_n bit to 1
0 = do nothing

3.8 Control and Status Register (CSR)

The default value of each CSR register bit on reset is shown just above the bit assignments.

bit 31	30	29	28	27	26	25	bit 24
0	0	0	x	x	x	x	x
CDI	CDIEN	BDIRQ	GA4	GA3	GA2	GA1	GA0

bit 23	22	21	20	19	18	17	bit 16
0	x	0	0	x	x	x	x
X	X	X	X	X	X	X	X

bit 15	14	13	12	11	10	9	bit 8
x	x	x	x	x	x	x	x
X	X	X	X	X	X	X	X

bit 7	6	5	4	3	2	1	bit 0
0	0	0	0	0	0	0	0
LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0

CDI: Change Detect Interrupt Status (R only)
1 = one or more ISR bits are set
0 = all ISR bits are low

CDIEN: Change Detect Interrupt Enable (R/W)
1 = assert hardware interrupt request whenever CDI is set
0 = CDI interrupt requests are disabled

BDIRQ: Board Interrupt Request (R only)
1 = DIO board is requesting an interrupt due to CDI, WI or EWI being set with the corresponding enable bit (CDIEN, WIEN, EWIEN) also set
0 = DIO board is not requesting an interrupt

GA4 – GA0: Geographical Address (R only)
These bits represent the physical slot (0 – 31) in which the DIO board resides.

X: Unused, don't care (R/W)

LED7 – LED1: Green LED outputs (R/W)
1 = LED is on (LEDn output pin is low)
0 = LED is off (LEDn output pin is high)

LED0: Red LED output (R/W)
1 = LED is on (LED0 output pin is low)
0 = LED is off (LED0 output pin is high)

3.9 Watchdog Control and Status Register (WDR)

The default value of each WDR register bit on reset is shown just above the bit assignments.

bit 31	30	29	28	27	26	25	bit 24
x	x	x	x	x	x	x	x
X	X	X	X	X	X	X	X

bit 23	22	21	20	19	18	17	bit 16
x	x	x	x	x	x	x	x
X	X	X	X	X	X	X	X

bit 15	14	13	12	11	10	9	bit 8
x	x	x	x	x	x	x	x
X	X	X	X	X	X	X	X

bit 7	6	5	4	3	2	1	bit 0
0	0	0	0	0	0	0	0
WI	WIEN	EWI	EWIEN	WREN	TS2	TS1	TS0

X: Unused, don't care (R/W)

WI: Watchdog Interrupt Status (R only)
1 = DIO board watchdog timer has expired
0 = DIO board watchdog timer has not expired

WIEN: Watchdog Interrupt Enable (R/W)
1 = DIO board is allowed to request an interrupt on WD timeout
0 = DIO board watchdog interrupt is disabled

EWI: Early Watchdog Interrupt Request (R only)
1 = DIO board early watchdog timer has expired
0 = DIO board early watchdog timer has not expired

EWIEN: Early Watchdog Interrupt Enable (R/W)
1 = DIO board is allowed to request an interrupt on EWD timeout
0 = DIO board watchdog interrupt is disabled

WREN: Watchdog Reset Enable (R/W)
1 = DIO board will be reset on WD timeout
0 = DIO board will not be reset on WD timeout

TS2 – TS0: Watchdog Timer Select (R/W)

TS2	TS1	TS0	Watchdog	Early Watchdog
0	0	0	126 ms	63 ms
0	0	1	252 ms	126 ms
0	1	0	504 ms	252 ms
0	1	1	1008 ms	504 ms
1	0	0	2016 ms	1008 ms
1	0	1	4032 ms	2016 ms
1	1	0	8064 ms	4032 ms
1	1	1	16,128 ms	8064 ms

3.10 Watchdog Clear Register (WCLR)

Since the WCLR register is write-only, there is no default value.

bit 31	30	29	28	27	26	25	bit 24
X	X	X	X	X	X	X	X

bit 23	22	21	20	19	18	17	bit 16
X	X	X	X	X	X	X	X

bit 15	14	13	12	11	10	9	bit 8
X	X	X	X	X	X	X	X

bit 7	6	5	4	3	2	1	bit 0
X	X	X	X	X	X	X	X

X: don't care (W only)
any value written to this register clears the WD and EWD timers

4. Functional Description

4.1 Edge Detectors

4.2 Interrupt logic

4.3 Watchdog Timer

5. Connector Pinout

The following table shows the pin assignments of the P2 (I/O) Connector of the ZPCI.4096-02 board.

	A	B	C	D	E	F
1	DIO_95	nc	nc	3.3V	3.3V	GND
2	DIO_90	DIO_91	DIO_92	DIO_93	DIO_94	GND
3	DIO_85	DIO_86	DIO_87	DIO_88	DIO_89	GND
4	DIO_80	DIO_81	DIO_82	DIO_83	DIO_84	GND
5	DIO_75	DIO_76	DIO_77	DIO_78	DIO_79	GND
6	DIO_70	DIO_71	DIO_72	DIO_73	DIO_74	GND
7	DIO_65	DIO_66	DIO_67	DIO_68	DIO_69	GND
8	DIO_60	DIO_61	DIO_62	DIO_63	DIO_64	GND
9	GND	GND	GND	GND	GND	GND
10	DIO_55	DIO_56	DIO_57	DIO_58	DIO_59	GND
11	DIO_50	DIO_51	DIO_52	DIO_53	DIO_54	GND
12	DIO_45	DIO_46	DIO_47	DIO_48	DIO_49	GND
13	DIO_40	DIO_41	DIO_42	DIO_43	DIO_44	GND
14	DIO_35	DIO_36	DIO_37	DIO_38	DIO_39	GND
15	DIO_30	DIO_31	DIO_32	DIO_33	DIO_34	GND
16	DIO_25	DIO_26	DIO_27	DIO_28	DIO_29	GND
17	DIO_20	DIO_21	DIO_22	DIO_23	DIO_24	GND
18	DIO_15	DIO_16	DIO_17	DIO_18	DIO_19	GND
19	DIO_10	DIO_11	DIO_12	DIO_13	DIO_14	GND
20	DIO_5	DIO_6	DIO_7	DIO_8	DIO_9	GND
21	DIO_0	DIO_1	DIO_2	DIO_3	DIO_4	GND
22	GA4	GA3	GA2	GA1	GA0	GND