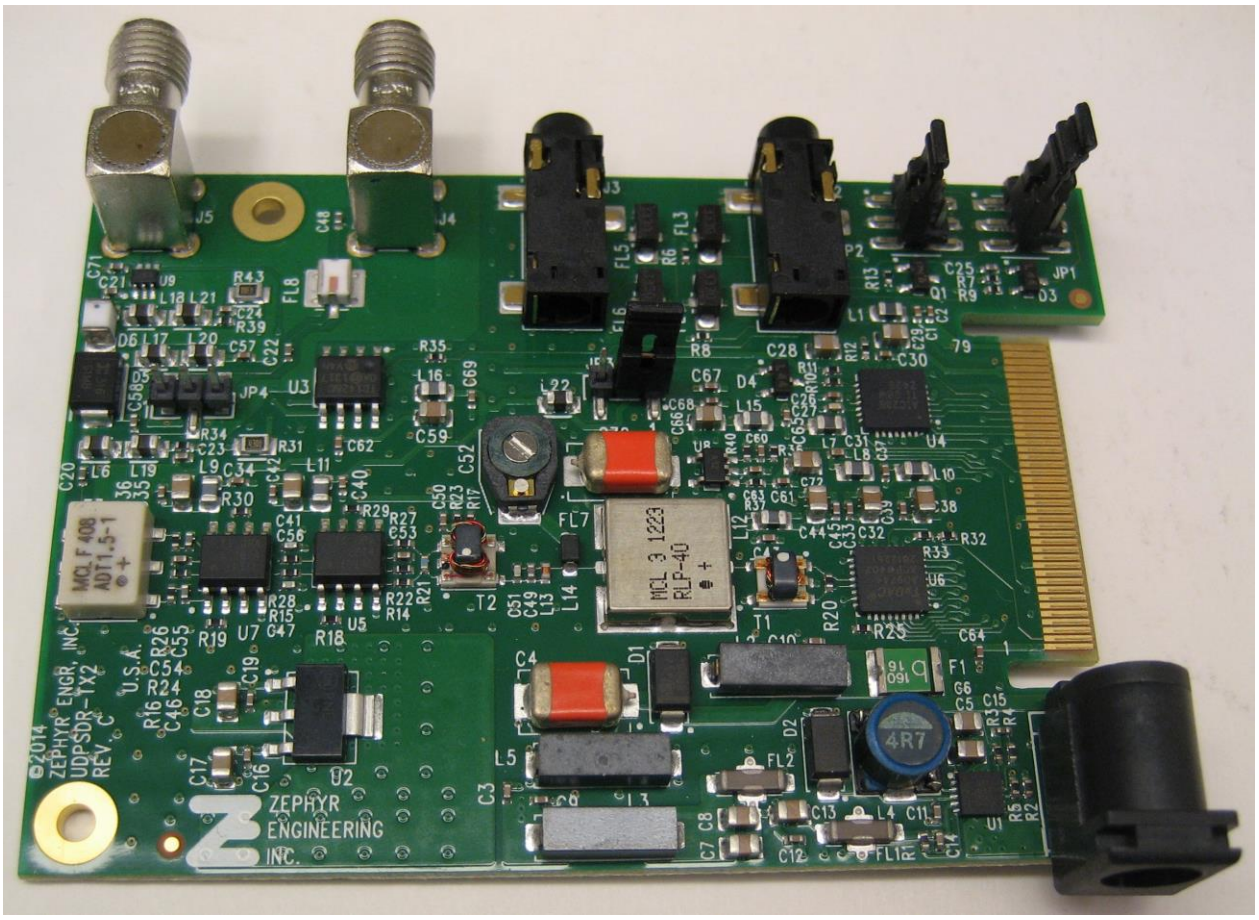
SDR Stick™

UDPSDR-TX2 Transmitter



User's Manual
Version 1.1 – 7 August 2014

Zephyr Engineering Inc.

1 Hardware Description

The following sections will help familiarize you with the setup and connections to your SDRstick™ TX2 SDR transmitter. The TX2 transmitter board is designed to work with the UDPSDR-HF2 receiver or the HSMCMEC-AD1 adapter board and an appropriate FPGA-based data engine (typically an Arrow BeMicroCV-A9 or SoCkit board). Note that while a BeMicroSDK will physically connect to an HF2/TX2 board set, there are insufficient resources in the BeMicroSDK FPGA to implement a transceiver.

1.1 UDPSDR-TX2 Connectors, Headers and Jumpers

See Figure 1 for UDPSDR-TX2 connector and jumper locations.

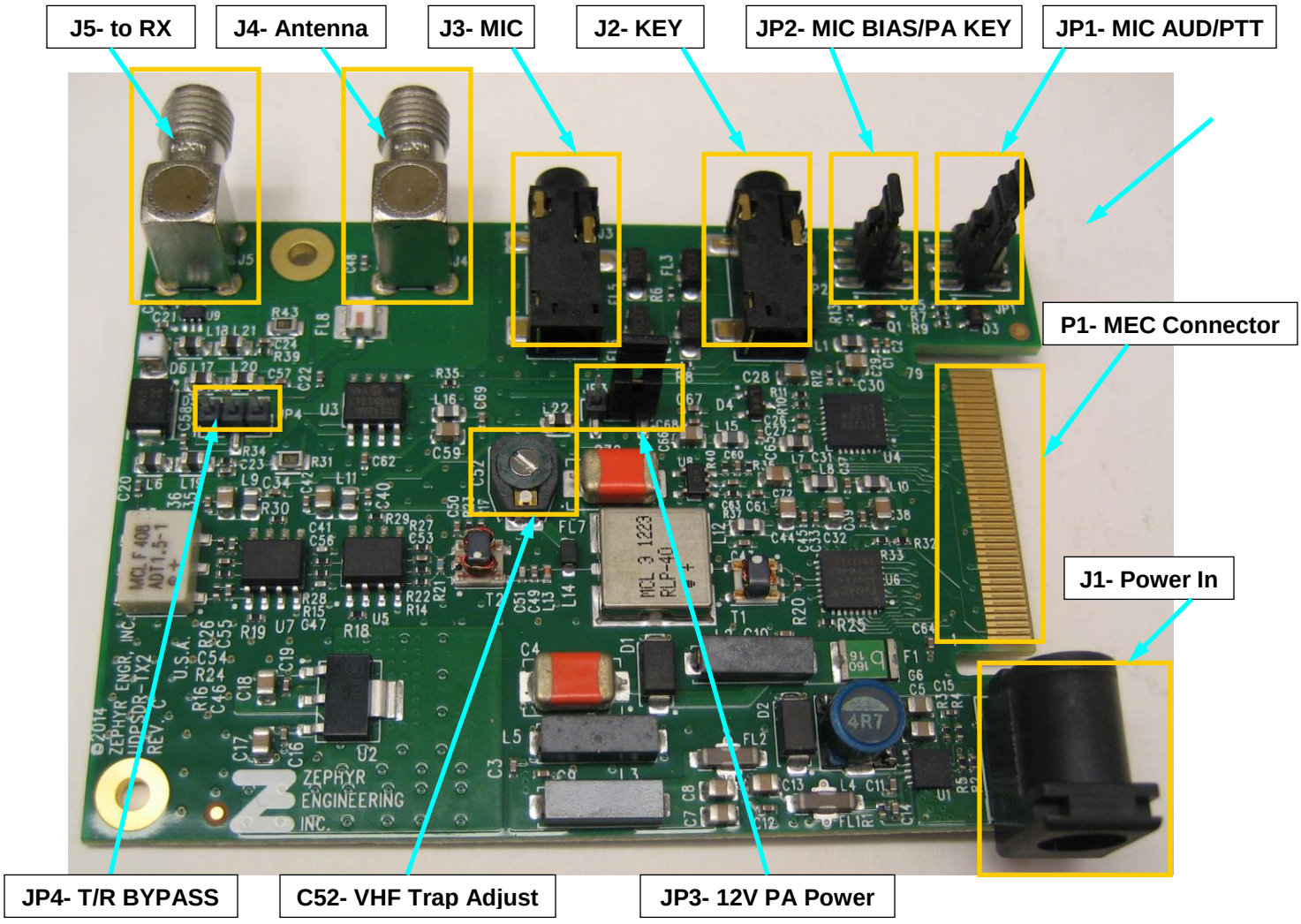


Figure 1 UDPSDR-TX2 Connectors and Jumpers

1.1.1 UDPSDR-TX2 Connectors

1.1.1.1 P1 – MEC connector

The P1 80-pin dual-sided MEC-style gold-finger edge connector plugs into either the J2 connector on the HF2 receiver (for use with the Arrow BeMicroCV-A9 FPGA development board) or the J1 connector on the HSMCMEC-AD1 adapter (for use with HSMC-equipped FPGA development boards, such as the Arrow SoCkit board). P1 connects digital data and power between the TX2 and the FPGA development board.

Note that the TX2 uses the BeMicroCV-A9 pin assignments, not the MEC connector pin assignments from the Samtec data sheet. P1 pin 1 is marked on TX2 by a “1” on the silkscreen. The pin 1 end is closest to the J1 power input connector. On HF2, J2 pin 1 is marked with a small dot on the silkscreen. On the AD1 adapter, J1 pin 1 is also marked with a small dot on the silkscreen. Two correct TX2 pairings are shown in Figure 2. Mechanical constraints only allow the TX2/HF2 and TX2/AD1 pairings to be made one way.

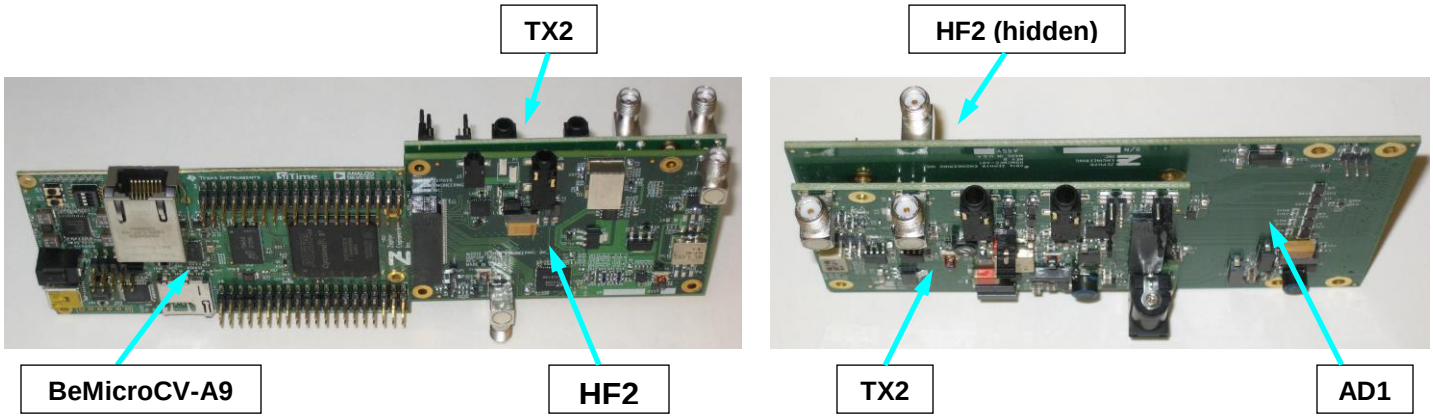


Figure 2 - Two correct TX2 configurations

1.1.1.2 J1 - Power In

Power is supplied to the transmitter in one of two ways, either from J1 (when TX2 is used with HF2 and the BeMicroCV-A9) or from the P1 MEC connector (when TX2 is used with the AD1 adapter).

1.1.1.2.1 Configuration 1: Use with BeMicroCV-A9

When TX2 is used with HF2 and the BeMicroCV-A9, 13.8V power is supplied to the transceiver system via J1. This is the case when TX2 is plugged directly into HF2. In this configuration, TX2 supplies 5V power to the BeMicroCV-A9 and the HF2 from its on-board switch-mode power supply (SMPS). TX2 uses a 12.0V on-board LDO linear regulator to power its power amplifier (PA). In this configuration, the power jacks on HF2 and BeMicroCV-A9 are not used. The combination of TX2, HF2 and BeMicroCV-A9 requires 12VDC at about 900mA. P1 mates with a 5.5mm x 2.1mm barrel plug (CUI part #PP3-002A, Digi-Key part #CP3-1000-ND). The center pin of P1 is positive.

1.1.1.2.2 Configuration 2: Use with SoCkit or other HSMC-equipped SDK

When TX2 is used with the AD1 adapter, 12.0V power comes from the HSMC power pins via the AD1 and MEC connector. In this case, J1, the TX2 SMPS and the TX2 12.0V LDO linear regulator are not used. The 5V power is supplied to the BeMicroCV-A9, HF2 and TX2 from the SMPS on the AD1. The TX2 Power Amplifier (PA) stage is powered directly from the HSMC 12.0V rail.

1.1.1.3 J2 – Key Input

Connect a straight key or paddle to J2, a 3.5mm stereo jack. Use the tip for the paddle dot contact, and the ring for the dash contact. Alternately, use the tip for a straight key and leave the ring unconnected. The sleeve is always ground.

1.1.1.4 J3 – Microphone Input

Connect a microphone to J3, a 3.5mm stereo jack. Jumpers on JP1 and JP2 route three signals to this connector: microphone audio input, microphone DC bias and PTT input. The default configuration is to put audio and bias on the tip and PTT on the ring. The sleeve is always ground. (See sections 1.1.2.1 and 1.1.2.2.) Most SDR software can source the microphone audio from the PC sound hardware. In this case, you can use this connector for PTT input only.

1.1.1.5 J4 – Antenna

The antenna is connected to J4, a standard SMA jack. This antenna is used for both transmit and receive, and is switched between the TX2 PA output while in transmit and the receiver RF connector (J5) while in receive.

1.1.1.6 J5 – Receiver RF

The receiver RF input is connected to J5, a standard SMA jack. During receive periods, the transmit/receive (T/R) switch passes signals from the antenna on J4 to this connector to supply RF to the receiver. Normally this is connected to the HF2 receiver input connector J5.

1.1.2 UDPSDR-TX2 Headers and Jumpers

1.1.2.1 JP1 – Microphone Audio and PTT Jumpers

Placing a 2mm jumper on JP1 pins 1-3 connects the microphone audio input to the J3 ring. Placing the jumper on JP1 pins 3-5 connects the microphone audio to the J3 tip. Placing a 2mm jumper on JP1 pins 2-4 connects the PTT input to the J3 ring. Placing the jumper on JP1 pins 4-6 connects PTT to the J3 tip. Pin 1 is marked by a white dot on the silkscreen. (Factory default is jumpers on pins 3-5 and 2-4.) See Table 1.

JP1 pin numbers	Microphone audio	PTT
1-3	J3 ring	-
3-5 (default)	J3 tip	-
2-4 (default)	-	J3 ring
4-6	-	J3 tip

Table 1 JP1 Jumper definitions

1.1.2.2 JP2 – Microphone Bias Jumper and PA Key Header

Placing a 2mm jumper on JP2 pins 1-3 connects the electret microphone bias to the J3 ring. Placing the jumper on JP2 pins 3-5 connects the bias to the J3 tip. The bias voltage is approximately 2.5V, and is fed to J3 through a 3300-ohm resistor. JP2 pins 4 and 6 are used to key an external power amplifier. The maximum open-circuit voltage on the PA key output (JP2-4) is 40V, and the maximum sink current should be kept under 200 mA. This output is open-drain, and is not pulled up by TX2 circuitry. Pin 1 is marked by a white dot on the silkscreen. (Factory default is a jumper on pins 3-5.) See Table 2.

JP2 pin numbers	Microphone bias	PA key function
1-3	J3 ring	-
3-5 (default)	J3 tip	-
2	-	GND
4	-	PA key output
6	-	GND

Table 2 JP2 Jumper Definitions

1.1.2.3 JP3 – PA Power Select Jumper

JP3 is used to select the power source of the PA. Placing a 2mm jumper on JP3 pins 1-2 connects 12V from the P1 MEC edge connector to power the PA when TX2 is powered from an AD1 adapter. Placing a 2mm jumper on JP3 pins 2-3 connects 12V from the on-board LDO regulator to power the PA when TX2 is plugged into an HF2 receiver and powered from J1. Pin 1 is marked by a white “1” on the silkscreen. (Factory default is a jumper on pins 1-2.) See Table 3.

JP3 pin numbers	PA power source	Configuration
1-2 (default)	Directly from P1 (MEC)	SoCkit/AD1
2-3	On-board 12V LDO powered from J1	BeMicroCV-A9

Table 3 JP3 Jumper Definitions

1.1.2.4 JP4 – T/R Switch Bypass Jumper

Placing a 2mm jumper on JP4 pins 1-2 or 2-3 bypasses the on-board T/R switch. The transmitter PA is connected to the J4 antenna connector. While the J5 connector can still be used to feed RF to the receiver, the transmitter PA is always connected. This will result in loss of receive sensitivity. This jumper should be used when the TX2 is operated below 1.8MHz, since the T/R switch will not switch full power below this frequency. When this jumper is installed, it is recommended to use off-board T/R switching. Pin 1 is marked by a white dot on the silkscreen. (Factory default is no jumpers installed.) See Table 4.

JP4 pin numbers	T/R switch function
1-2	Bypass T/R switch
2-3	Bypass T/R switch
None (default)	Normal T/R switch operation

Table 4 – JP4 Jumper Definitions

2 UDPSDR-TX2 Theory of Operation

The UDPSDR-TX2 PCB block diagram is shown in Figure 3. The signal flow is straightforward, with the RF signal generated by the DAC passing through the reconstruction filter, PA, T/R switch and LPF.

The DAC clock and DAC data inputs are generated by the FPGA. A digital PWM output from the FPGA is buffered and low-pass filtered and used to set the DAC output level.

The audio CODEC can be used to capture microphone audio, or the PC sound system can be used for this purpose. PTT and paddle/straight key inputs are sent directly to the FPGA.

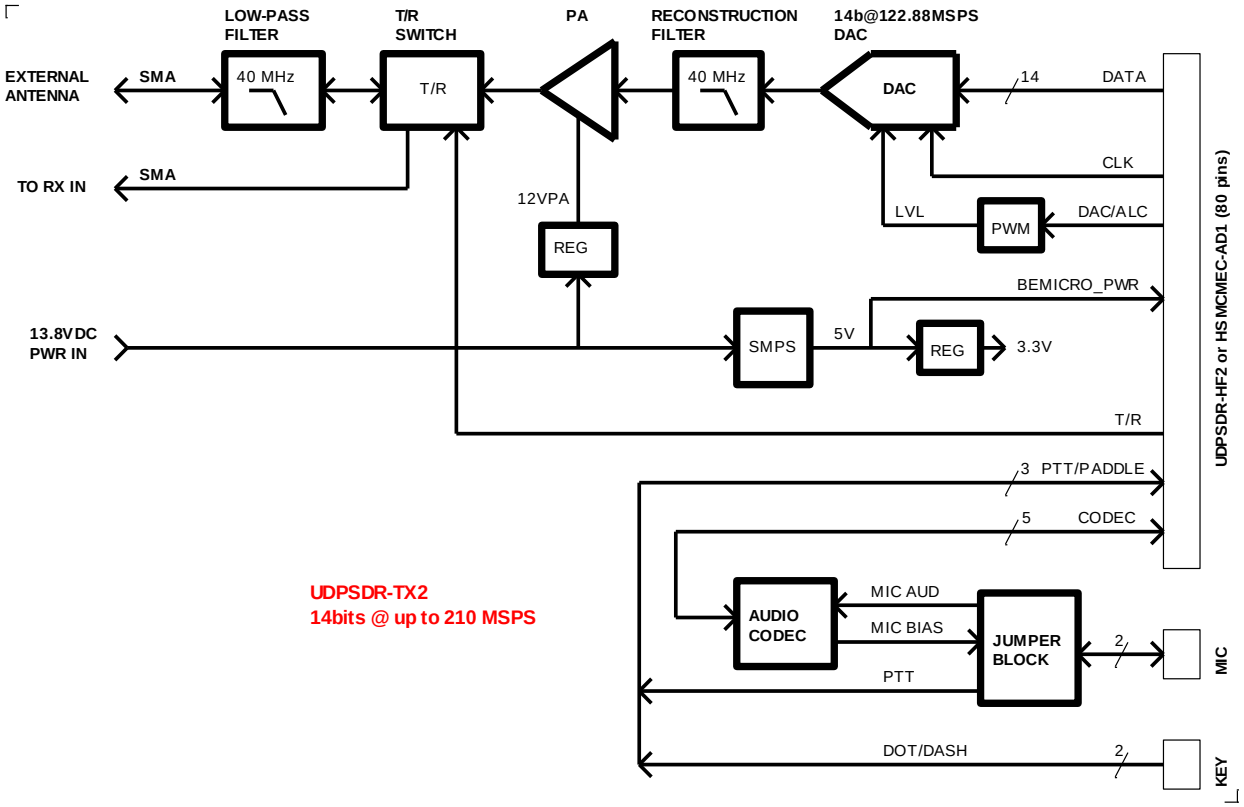


Figure 3 - UDPSDR-TX2 Hardware Block Diagram

3 Specifications

- Frequency Range: 200kHz to 55MHz, Digital Up Conversion (DUC)
- Input impedance: 50 ohms
- RF output power: 500mW typical (300mW typical at 54MHz)
- Sampling Width and Rate: 14bits @ up to 210Msps
- Antenna connection: standard SMA
- Power consumption: +13.8VDC @ 900mA typical (incl BeMicroCV-A9 and HF2)
- Dimensions, UDPSDR-TX2: 56mm x 80mm (2.2”W x 3.3”L)
- Dimensions, including BeMicroCV-A9 and HF2: 56mm x 177mm (2.2”W x 7.0”L)

Appendix A – UDPSDR-TX2 P1 Pin Definitions

P1 Pin	Signal Name	P1 Pin	Signal Name
1	3.3V power in	2	3.3V power in
3	DAC_CLK	4	n/c
5	n/c	6	n/c
7	n/c	8	FPGA_PTT_N
9	n/c	10	GND
11	n/c	12	EN_RX_ANT
13	n/c	14	PA_KEY
15	n/c	16	DAC_ALC
17	n/c	18	DACD13
19	n/c	20	DACD12
21	GND	22	GND
23	n/c	24	DACD11
25	n/c	26	DACD10
27	n/c	28	DACD9
29	n/c	30	DACD8
31	n/c	32	GND
33	GND	34	DACD7
35	n/c	36	DACD6
37	n/c	38	DACD5
39	n/c	40	DACD4
41	n/c	42	DACD3
43	n/c	44	GND
45	MIC_CDOUT	46	DACD2
47	n/c	48	DACD1
49	n/c	50	DACD0
51	n/c	52	CMCLK
53	GND	54	GND
55	CDIN	56	n/c
57	MIC_CODEC_nCS	58	FPGA_DASH_N
59	CBCLK	60	n/c
61	CLRCIN	62	SPI_DATA
63	CLRCOUT	64	SPI_CLK
65	n/c	66	n/c
67	n/c	68	n/c
69	n/c	70	n/c
71	+12V PA power in	72	n/c
73	+12V PA power in	74	n/c
75	n/c	76	GND
77	n/c	78	FPGA_DOT_N
79	5.0V power out	80	5.0V power out

3.3V – logic power input

DAC_CLK – AD9744 DAC clock input

FPGA_PTT_N – active-low output from tip or ring contact of microphone jack J3

EN_RX_ANT – active-high T/R switch control input pin (1=receive, 0=transmit)

PA_KEY – active-high PA-KEY input pin (1=PA_KEY grounded, 0=PA_KEY open

DAC_ALC – AD9744 DAC PWM REFIO level control input pin

DACD[13:0] – AD9744 DAC data input pins

MIC_CDOUT – TLV320AIC23B DOUT output pin

CMCLK – TLV320AIC23B XTI/MCLK input pin

CDIN – TLV320AIC23B DIN input pin

MIC_CODEC_nCS – TLV320AIC23B CSn input pin

FPGA_DASH_N – active-low output from ring contact of paddle jack J2

CBCLK – TLV320AIC23B BCLK input pin

CLRCIN - TLV320AIC23B LRCIN input pin

SPI_DATA – TLV320AIC23B SDIN input pin

CLRCOUT - TLV320AIC23B LRCOUT input pin

SPI_CLK – TLV320AIC23B SCLK input pin

+12V – PA power input when JP3 pins 1-2 are jumpered, else not used

FPGA_DOT_N – active-low output from tip contact of paddle jack J2

GND – system ground and power return

5.0V – power out to BeMicroCV-A9 and HF2 from on-board SMPS

Note: All signal directions are referenced to the UDPSDR-TX2 transmitter.