Zephyr Engineering, Inc.

User's Manual, ZPC.1900, Rev. B

Rev 1.2

23 June, 2003

Preliminary

The information presented within this manual is preliminary and is subject to change without notice.

1. Introduction

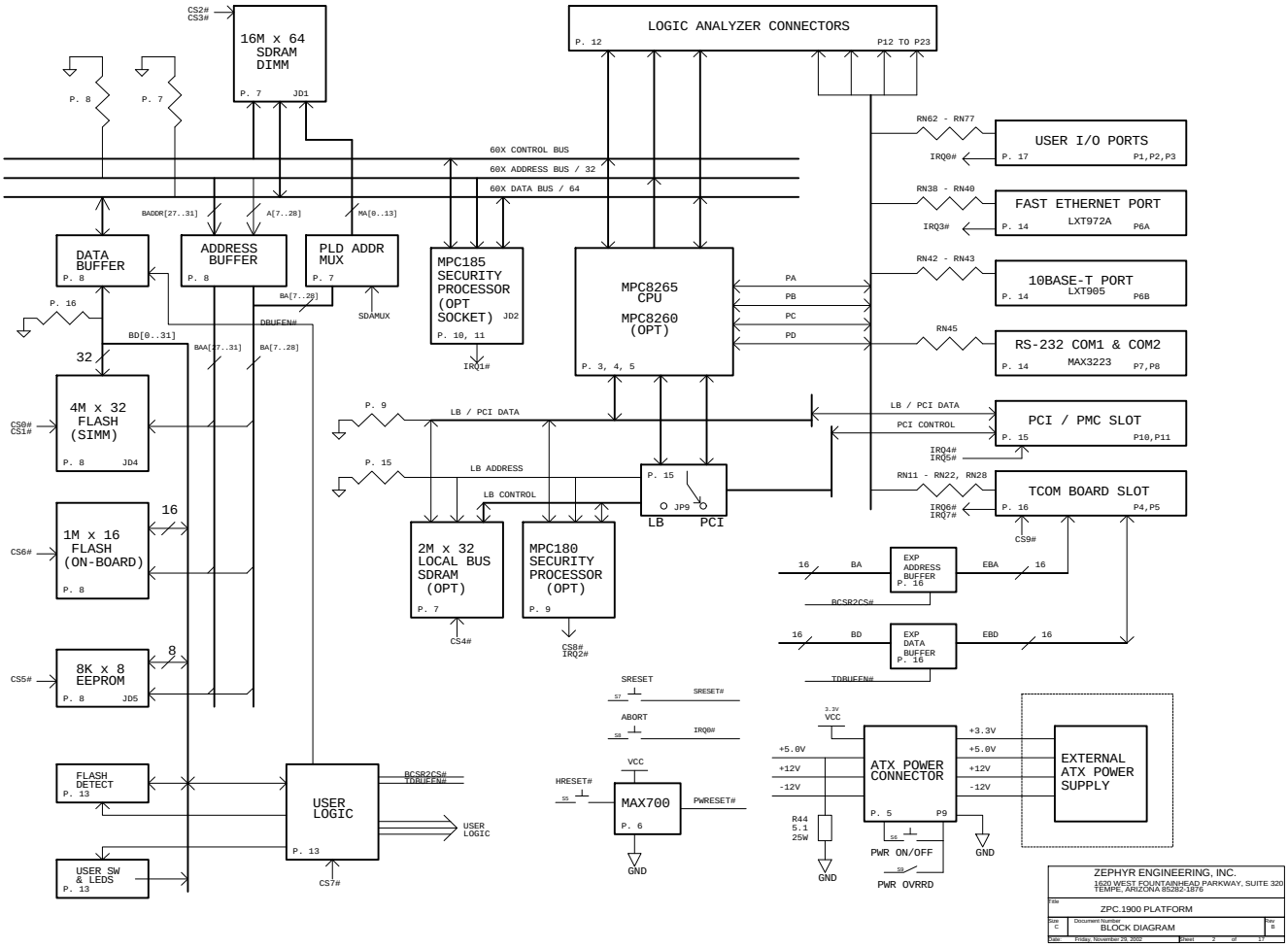
Zephyr Engineering's ZPC.1900 Security Processor Development Platform is an ATX form-factor Single Board Computer featuring a PowerPC MPC8265 CPU. This feature rich platform provides a versatile environment for evaluation, development and demonstration of many members of the Motorola Security Processor family. On board are two Security Processors, the MPC185 and MPC180. Additional Security Processors are supported via a 32 bit 66/33 MHz PMC slot. Optional PMC plug in modules for the MPC190 and MPC184 may be purchased from Zephyr Engineering. For more information on these products please visit: www.zpci.com.

2. ZPC.1900 Features and Setup

2.1 Feature List

- MPC8265 CPU – 266 MHz
- MPC185 Security Processor
- MPC180 Security Processor
- 64 MB of 64 Bit SDRAM
- 4 MB Flash SIMM
- 2 MB On-Board Flash Boot Rom
- 8 KB EEPROM
- 8 MB Local Bus SDRAM
- 2 Ethernet Ports – 1 10/100BaseT, 1 10BaseT
- 2 RS232 Ports
- 32 Bit 66/33 MHz PMC Slot
- JTAG Connector for MPC8265 On-Chip Debug Port
- Interrupt Status LEDs
- User Defined LEDs
- User Defined Switches
- High Speed Logic Analyzer Connectors (AMP Mictor)
- Standard ATX Form-factor
- Uses Standard ATX Power Supply

2.2 Block Diagram



2.2.1 MPC8265

The MPC8265 is a member of the PowerQuicc II communications processor family. This CPU features:

- MPC603e core
- Core frequencies up to 266 MHz
- Separate 16Kbyte instruction and data caches
- 64 bit data, 32 bit address 60x bus
- Selectable PCI or MPC8260 style Local bus
- Integrated memory controller
- Communications Processor Module

2.2.2 SDRAM

The ZPC.1900 provides a standard 168 pin DIMM socket for memory expansion. The standard platform ships with 64 MB of SDRAM.

2.2.3 Boot Flash

A 2 Mbyte AMD Am29F016 2Mx8 Flash ROM is provided. Boot code shipped with the board contains a minimal debugger and either a VxWorks image bootloader or UBOOT for Linux.

2.2.4 Flash SIMM

On board is an 80 pin SIMM socket for a Flash DIMM module. The socket allows up to 16MB Flash modules to be used. A 2M x 32 (8 Mbyte) module is provided with the ZPC.1900 platform.

2.2.5 Security Processors

Two Motorola Security Processors are featured on the ZPC.1900 board.

- MPC185 – The ZPC.1900 is configured in multi-master mode for the 60x bus, allowing optimum performance for security applications.
- MPC180 - In Local Bus Mode a Motorola MPC180 Security Processor is connected to the local bus side of the MPC8265.

2.2.6 PMC Slot

In PCI Mode, a 32 Bit 66/33 MHz PMC slot is available. General purpose PMC IO boards or additional Security Processors such as the MPC190 on Zephyr Engineering's ZPCI.3900 or the MPC184 (ZPCI.3901) may be used in this slot.

2.2.7 EEPROM

An 8Kx8 Atmel AT28HC64B EEPROM is provided for non-volatile user parameter storage.

2.2.8 Ethernet

The MPC8265's embedded Communication Processor Module (CPM) hosts 2 ethernet controllers. Physical interfaces and magnetics are implemented on the ZPC.1900 board. For the 10/100 Fast Ethernet port an LXT972 interface is used. For the 10BASET port the physical interface is an LXT905.

2.2.9 RS-232

Two RS-232 ports are driven from the MPC8265's Serial Communications Controller to an on board RS-232 level translator.

2.2.10 TCOM Expansion Slot

This port is for future expansion.

2.2.11 User IO Expansion Port

Many of the MPC8265 control and CPM signals are pinned out to a User IO port consisting of three 96 pin DIN type connectors. These may be used by users for additional hardware prototyping.

2.3 Hardware Setup

The ZPC.1900 ships with default configuration options that make it usable right out of the box for most users. This section describes the options that will most commonly be modified or referred to by a user.

2.3.1 Power Supply

The ZPC.1900 uses a standard PC ATX power supply. The power supply connects to the board at P9. See section 7.20 for P9 pin definitions.

Many ATX power supplies require a load on the +5VDC power that exceeds the minimal amount of current consumed by the ZPC.1900. For platforms that have no other connections to the power supply and use little or no current on +5VDC, a power load resistor is provided on the board. The load resistor is enabled by placing a jumper on JP17.

2.3.2 Console Port

Two RS-232 Serial ports are provided on the ZPC.1900 at P7. The upper connector is defined to be the console port by the on board boot rom. This connector is a standard 9 pin male D-Sub connector and has the same pin out as a standard PC serial port. Transmit data out TXD is on pin 3 and receive data in RXD is on

pin 2. Ground is on pin 5. A null modem (cross over) cable is required to connect the platform to a standard PC serial port.

2.3.3 Memory Requirements

Standard 168 pin, 64 Bit SDRAM DIMMs are used in socket JD1. A 64 MB SDRAM DIMM is provided with the board.

2.3.4 PCI or Local Bus Mode Selection

The MPC8265 and ZPC.1900 board may be configured to operate in one of two modes:

1. PCI Bus Mode
2. Local Bus Mode

By default, the PCI Bus Mode is configured at the factory.
Each mode hosts certain features that are available only when the CPU and the ZPC.1900 board are configured for that mode. The table below defines these features.

Function/Device	Available in Mode
60x Bus SDRAM (main memory)	Both
2 MB On-board Boot Rom Flash	Both
8 MB Flash SIMM	Both
8 KB EEPROM	Both
Board Control/Status Registers	Both
MPC185 Security Processor	Both
8 MB Local Bus SDRAM	Local Bus
MPC180 Security Processor	Local Bus
TCOM Expansion Slot	Local Bus
PMC PCI Slot	PCI Bus

In addition to software that must initialize the MPC8265, the ZPC.1900 board configuration must match the mode being selected. The following options/jumpers/switches vary according to the option being configured:
1. Reset Configuration Word (programmed into boot flash)
2. User Clock Configuration Switches (S4)
3. PCI / Local Bus Select Jumper (JP9)

2.3.5 MPC8265 Clock Configuration

The MPC8265 supports a large number of clock frequency configurations (see the MPC8260 User Manual, Section 9 as well as the PCI Bridge Functional Specification Addendum). This configuration is accomplished by sampling the MODCK pins at reset and when in local bus mode by reading designated bits of the reset configuration word from the boot rom. Some of the MODCK pins are user configurable via the switches at S4. Other pins are set by zero ohm option resistors that may be populated or de-populated on the board. The table below shows the default configuration of the ZPC.1900. The default configuration may be too conservative for users wishing to demonstrate performance or run benchmarks. For users who may be connecting and debugging prototype hardware to the platform, the default settings may be too aggressive. Alternate configurations are also shown below.

Clock Configurations

MODE	Input Clock Frequency (Bus Clock)	CPM Frequency	CPU Core Frequency	MODCK_H Set by option resistors in PCI MODE. Set by RSTCONF in LB MODE	MODCK[1-3] Set by S4[2-4]
PCI MODE	66 MHz	133 MHz	166 MHz	0000 Configuration Resistors	000 [ON-ON-ON]
Local Bus MODE	66 MHz	133 MHz	133 MHz	0x05 from Reset Configuration Word	101 [OFF-ON-OFF]
PCI MODE	66 MHz	200 MHz	266 MHz	0000 Configuration Resistors	111 [OFF-OFF-OFF]
Local Bus MODE	66 MHz	133 MHz	266 MHz	0x06 from Reset Configuration Word	001 [ON-ON-OFF]
Local Bus MODE	33 MHz	133 MHz	233 MHz	0x02 from Reset Configuration Word	010 [ON-OFF-ON]

Please note that to change the Bus Clock it is necessary to change the main oscillator on the board. The ZPC.1900 supports this by using a socketed oscillator. There are two types of commonly available DIP oscillators. Both the 8 pin DIP and the 16 pin DIP size oscillators are supported. Also note that if any CPM frequency other than 133 MHz is selected, changes will also need to be done to the boot rom code to provide the correct baud rate input to the console port.

2.3.6 Jumper Definitions

The functions of configuration jumpers are described in the following table.

Jumper	Jumper Name	Default	Pins	Functional Description
JP3	LB SDRAM ENABLE	X	open	enable clock to local bus SDRAM
			shorted	disable clock to local bus SDRAM
JP6	GROUND CONNECTION	X	open	float logic ground from chassis ground
			shorted	connect logic ground to chassis ground
JP8	PCI CLK SEL	X	open	66MHz PCI clock
			shorted	33MHz PCI clock
JP9	PCI/LB SEL	X	1-2	Select PCI Bus Mode
			2-3	Select Local Bus Mode
JP12	ENDIAN CONTROL		1-2	0 -> MPC180 Endian control pin
			3-4	1 -> MPC180 Endian control pin
		X	5-6	PA1 -> MPC180 Endian control pin
			7-8	LA17 -> MPC180 Endian control pin
JP14	CS0# BOOT SELECT	X	1-3 2-4	Boot from on-board 2MB FLASH
			1-2 3-4	Boot from 8MB FLASH SIMM
JP17	ENABLE 5V 1A LOAD	X	open	disconnect 5 ohm load
			shorted	connect 5 ohm load to 5V bus

2.4 Software Setup

2.4.1 Default Memory Map

Device	Recommended Address
Main Memory – 64 MB	**0x00000000 – 0x03FFFFFF**
Local Bus SDRAM – 8MB	**0x04000000 – 0x047FFFFF****
MPC180	**0x05000000 – 0x05FFFFFF****
Board Control/Status Registers	**0x21000000 – 0x2100FFFF**
8KB EEPROM	**0x22000000 – 0x2200FFFF**
MPC185	**0x30000000 – 0x37FFFFFF**
PMC Slot	**0x60000000 – 0x6FFFFFFF**
8MB SIMM Flash	**0xE0000000 – 0xE0FFFFFF**
2MB on-board Boot Flash	**0xFE000000 – 0xFFFFFFFF**

** These devices are not available in the default PCI Bus Mode configuration

2.4.2 Boot Flash

The on-board boot rom contains a minimal debugger and bootloader.
It is also possible to boot from the Flash SIMM module. The ZPC.1900 ships with a copy of the on-board flash boot rom image programmed onto the Flash SIMM module. This provides a backup should the on-board copy be accidentally erased or corrupted. To boot from the SIMM module simply change the direction of the two jumpers on JP14 from both horizontal to both vertical. The default position of both horizontal connects chip select CS0 to the on board flash and CS6 to the Flash SIMM module. The alternate jumper position reverses these connections, connecting CS0 to the Flash SIMM module and CS6 to the on-board flash.

3. Connector Definitions

The ZPC.1900 contains 39 connectors. The function of each connector is listed in the following table.

Number	Name	Type	Functional Description
JD1	EXPANDABLE SDRAM	168-pin DIMM	System Memory
JD2	MPC185	256-pin BGA	Security Processor
JD3	CLK OSC	14-pin DIP	Provides Bus Clock to CPU
JD4	EXPANDABLE FLASH	80-pin SIMM	Boot Flash backup + parameter storage
JD5	EPROM(8Kx8)	PLCC-32	Stores System Boot Parameters
JP1	G/P USER LOGIC	20-pin dual-row 2mm pitch	HW prototyping resource
JP2	LOGIC JTAG	10-pin dual-row 0.1" pitch	PLD Programming header
JP4	LXT972A JTAG	8-pin dual-row 0.1" pitch	JTAG
JP5	SYSTEM RESET	2-pin 2mm pitch	In parallel with S5
JP7	PMC JTAG	8-pin sgl-row 0.1" pitch	JTAG for PMC board
JP10	MPC826x JTAG	16-pin dual-row 0.1" pitch	Emulator connection
JP11	MPC185 JTAG	10-pin dual-row 0.1" pitch	Component JTAG
JP13	MPC180 JTAG	10-pin dual-row 0.1" pitch	Component JTAG
JP15	POWER ON/OFF	2-pin 2mm pitch	In parallel with S6
JP16	POWER ON OVERRIDE	2-pin 2mm pitch	In parallel with S9
P1	USER IO PORT	96-pin DIN - F	HW prototyping resource
P2	USER IO PORT	96-pin DIN - F	HW prototyping resource
P3	USER IO PORT	96-pin DIN - F	HW prototyping resource
P4	TCOM PORT P1	128-pin DIN - F	Future Expansion
P5	TCOM PORT P2	128-pin DIN - F	Future Expansion
P6A	10BASE-T	RJ-45	10BT Ethernet
P6B	FAST ETHERNET	RJ-45	100BT Ethernet
P7A	COM1 (upper)	DB-9M	Console Port
P7B	COM2 (lower)	DB-9M	2nd RS-232 Port
P9	POWER SUPPLY CONNECTOR	20-pin male ATX	ATX Power Supply input
P10	PMC CARD P10	64-pin PMC	PMC board slot
P11	PMC CARD P11	64-pin PMC	PMC board slot
P12	MPC LOGIC ANALYZER	38-pin MICTOR	60x Bus Address
P13	MPC LOGIC ANALYZER	38-pin MICTOR	60x Bus Data (high) [0-31]
P14	MPC LOGIC ANALYZER	38-pin MICTOR	60x Bus Data (low) [32-63]
P15	MPC LOGIC ANALYZER	38-pin MICTOR	60x Bus Control Signals
P16	MPC LOGIC ANALYZER	38-pin MICTOR	CPU Chip select and Interrupts
P17	MPC LOGIC ANALYZER	38-pin MICTOR	Port A signals
P18	MPC LOGIC ANALYZER	38-pin MICTOR	Port B signals
P19	MPC LOGIC ANALYZER	38-pin MICTOR	Port C signals
P20	MPC LOGIC ANALYZER	38-pin MICTOR	Port D signals
P21	LB/PCI LOGIC ANALYZER	38-pin MICTOR	Local Bus Data / PCI Address/Data Bus
P22	LB/PCI LOGIC ANALYZER	38-pin MICTOR	Local Bus Address/ PCI control signals
P23	LB/PCI LOGIC ANALYZER	38-pin MICTOR	PCI control + clock configuration

Switches and Debug Functions

There are 9 switches on the ZPC.1900. The function of each switch is listed in the following table.

Number	Name	Type	Functional Description
S1	USER SETTING	DIP-8	User defined – read by software at 0x21000001
S2	USER CHIP SELECT ISOLATION	DIP-8	For debugging, each CS may be isolated from CPU
S3	USER CHIP SELECT ISOLATION	DIP-8	For debugging, each CS may be isolated from CPU
S4	USER CLOCK CONFIG	DIP-8	Configures CPU clock ratios
S5	SYSTEM RESET	PBT-mom	Connects to CPU HRESET#
S6	POWER ON/OFF	PBT-mom	Controls power supply on/off
S7	SOFT RESET	PBT-mom	Connects to CPU SRESET#
S8	ABORT	PBT-mom	Connects to MPC8265 IRQ0
S9	POWER ON OVERRIDE	toggle	Bypass on-board power switch logic to use power switch on power supply

3.1 S1 – User Setting Switches

The state of these user defined switches can be read from the User Switches register at 0x21000001.

3.2 S2, S3 – User Chip Select Isolation

Each of the Chip Selects driven from the MPC8265 memory controller passes through a user configurable chip select isolation switch. For debugging purposes, individual chip selects may be isolated from the CPU by setting the appropriate switch to the OFF position. The default configuration is all switches ON.

Switch	Chip Select	Device
S2-1	CS0	Boot Flash
S2-2	CS1	Reserved for Flash Expansion
S2-3	CS2	SDRAM
S2-4	CS3	Reserved for SDRAM Expansion
S2-5	CS4	Local Bus SDRAM
S2-6	CS5	EEPROM
S2-7	CS6	Flash SIMM
S2-8	CS7	Board Control/Status Registers
S3-1	CS8	MPC180
S3-2	CS9	TCOM Expansion Slot
S3-3	CS10	Not Used
S4-4	CS11	Not Used
S4-5	None	Not Connected
S4-6	None	Not Connected
S4-7	None	Not Connected

3.3 S4 - User Clock Configuration

Switch S4 is used to set user clock configuration settings shown in the following table. See section 2.3.5 for alternate configuration possibilities.

Switch	Name	Local Bus Mode	PCI Bus Mode (default)
S4-1	not used	off	off
S4-2	MODCK1	off	on
S4-3	MODCK2	on	on
S4-4	MODCK3	off	on
S4-5	not used	off	off
S4-6	not used	off	off
S4-7	not used	off	off
S4-8	RSTCONF	on	on

3.4 S5 – System Reset

Switch S5 is debounced and used to drive both HRESET# and PWRESET# to the MPC8265.

3.5 S6 – Power On/Off

Switch S6 is debounced to generate a control signal that is used to turn the power supply on / off.

3.6 S7 – Soft Reset

Switch S7 is a momentary normally open contact connecting to the MPC8265 Soft Reset signal.

3.7 S8 – Abort

S8 is a normally open switch connecting to IRQ0.

3.8 S9 – Power On Override

For some users it is preferable to use the switch on the ATX power supply or to use a switch on an external power strip rather than the switch on the ZPC.1900 to turn power on and off. For this function S9 is provided to bypass the power control logic on the ZPC.1900.

4. LED Functions

There are 9 LED assemblies on the ZPC.1900. The function of each LED is listed in the following table.

Number	Name	Type	Functional Description
LED1	USER LEDS	4-stack RED	top = bit 7 (MSB); bottom = bit 4
LED2	USERLEDS	4-stack GRN	top = bit 3; bottom = bit 0 (LSB)
LED3	10BASE STATUS	3-stack R-Y-G	R=TX; Y=RX; G=Link
LED4	FAST ETHERNET STATUS	3-stack R-Y-G	R=?; Y=?; G=?
LED5	POWER	Board edge GRN	On = +5V active
LED6	ACTIVE	smt GRN	Driven by 60x Bus DBB# signal
LED7	DEBUG	smt YEL	Driven by QREQ# signal
LED8	MPC185-INT	smt YEL	MPC185 interrupt asserted
LED9	MPC180-INT	smt YEL	MPC180 interrupt asserted

5. Connector Pinouts

5.1 JD1 – Expandable SDRAM DIMM Connector Pinout

Pin Number	Signal	Pin Number	Signal	Pin Number	Signal	Pin Number	Signal
1	GND	48	WE#	95	D40	142	D51
2	D0 (MSB)	49	3.3V	96	GND	143	3.3V
3	D1	50	NC	97	D41	144	D52
4	D2	51	NC	98	D42	145	NC
5	D3	52	NC	99	D43	146	NC
6	3.3V	53	NC	100	D44	147	NC
7	D4	54	GND	101	D45	148	GND
8	D5	55	D16	102	3.3V	149	D53
9	D6	56	D17	103	D46	150	D54
10	D7	57	D18	104	D47	151	D55
11	D8	58	D19	105	NC	152	GND
12	Gnd	59	3.3V	106	NC	153	D56
13	D9	60	D20	107	GND	154	D57
14	D10	61	NC	108	NC	155	D58
15	D11	62	NC	109	NC	156	D59
16	D12	63	CKE	110	3.3V	157	3.3V
17	D13	64	GND	111	CAS#	158	D60
18	3.3V	65	D21	112	WE4#	159	D61
19	D14	66	D22	113	WE5#	160	D62
20	D15	67	D23	114	CS2#	161	D63
21	NC	68	GND	115	RAS#	162	GND
22	NC	69	D24	116	GND	163	CK3
23	GND	70	D25	117	MA1	164	NC
24	NC	71	D26	118	MA3	165	SA0
25	NC	72	D27	119	MA5	166	SA1
26	3.3V	73	3.3V	120	MA7	167	SA2
27	WE#	74	D28	121	MA9	168	3.3V
28	WE0#	75	D29	122	MA12		
29	WE1#	76	D30	123	MA11		
30	CS2#	77	D31	124	3.3V		
31	NC	78	GND	125	CK1		
32	GND	79	CK2	126	GND		
33	MA0	80	NC	127	GND		
34	MA2	81	NC	128	CKE		
35	MA4	82	SDA	129	CS3#		
36	MA6	83	SCL	130	WE6#		
37	MA8	84	3.3V	131	WE7#		
38	MA10	85	GND	132	GND		
39	MA13	86	D32	133	3.3V		
40	3.3V	87	D33	134	NC		
41	3.3V	88	D34	135	NC		
42	CLK0	89	D35	136	NC		
43	GND	90	3.3V	137	NC		
44	NC	91	D36	138	GND		
45	CS2#	92	D37	139	D48		
46	WE2#	93	D38	140	D49		
47	WE3#	94	D39	141	D50		

5.2 JD3 – Clock Oscillator Pinout

The oscillator socket at JD3 is wired to accept either an 8 pin or 14 pin Dual-Inline-Package component. The following table shows the pinout for the 16 pin socket.

Pin Number	Signal
1	Output Enable**
2	NC
3	NC
4	GND
5	NC
6	NC
7	GND
8	OUTPUT
9	NC
10	NC
11	OUTPUT
12	NC
13	NC
14	3.3V

**Output Enable is pulled up on the board.

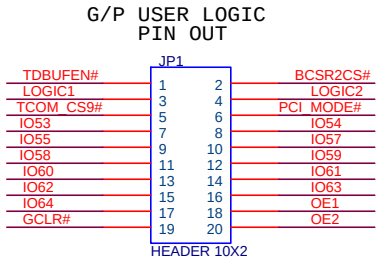
5.3 JD4 – Expandable FLASH SIMM Socket Pinout

Pin Number	Signal	Pin Number	Signal
1	GND	41	A18
2	+5V	42	A19
3	VPP (+5V)	43	A20
4	OE#	44	A21
5	WE0#	45	A22
6	WE1#	46	A23
7	RESET#	47	A24
8	D23	48	A25
9	D22	49	A26
10	D21	50	A27
11	D20	51	A28
12	D19	52	A29
13	D18	53	WE3#
14	D17	54	GND
15	D16	55	D8
16	D31	56	D9
17	D30	57	D10
18	D29	58	D11
19	D28	59	D12
20	D27	60	D13
21	NC	61	D14
22	NC	62	D15
23	CS1#	63	D0
24	CS6# **	64	D1
25	GND	65	D2
26	D26	66	D3

27	D25	67	D4
28	D24	68	D5
29	WE2#	69	D6
30	A7	70	D7
31	A8	71	VPP (+5V)
32	A9	72	+5V
33	A10	73	PD1
34	A11	74	PD2
35	A12	75	PD3
36	A13	76	PD4
37	A14	77	PD5
38	A15	78	PD6
39	A16	79	PD7
40	A17	80	GND

5.4 JP1 – General Purpose User Logic Header Pinout

JP1 may be used to monitor the state of control signals connecting to the User Logic PLD U1 and/or to add future capabilities. The "IOxx" signals connect to the PLD and are currently unused.



5.5 JP2 – Logic JTAG Header Pinout

JP2 is used to program both the User Logic PLD (U1) and the SDRAM multiplexer PLD U10. Both components are Altera CPLD parts and are programmed with the Altera ByteBlaster cable. The following table shows the pinout for JP2.

Pin	Name	Functional Description
1	TCK	JTAG Clock Signal
2	GND	Ground
3	TDO	JTAG Data Out (from SDRAM multiplexer)
4	+5V	Power
5	TMS	JTAG TMS
6	NC	No Connection
7	GND	Ground
8	NC	No Connection
9	TDI	JTAG Data In (to user pld)
10	GND	Ground

5.6 JP4 – LXT972A JTAG Header Pinout

The following table shows the pinout of the LXT972A JTAG header (JP4).

Pin	Name	Functional Description
1	TRST_L	LXT972 pin 31
2	ground	power ground
3	TCK	LXT972 pin 30
4	ground	power ground
5	TMS	LXT972 pin 29
6	ground	power ground
7	TDO	LXT972 pin 28
8	TDI	LXT972 pin 27

5.7 JP5 – System Reset Header Pinout

The following table shows the pinout of the Reset header (JP5).
JP5 is intended to be used for an external reset switch, such as on an ATX system chassis

Pin	Name	Functional Description
1	reset	low causes reset assertion; logic holds low for 500 ms
2	ground	power ground

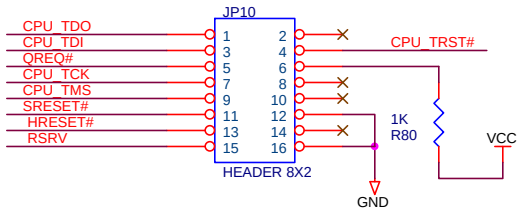
5.8 JP7 – PMC JTAG Header Pinout

The following table shows the pinout of the PMC JTAG connector (JP7).

Pin	Name	Functional Description
1	+3.3V	+3.3V power
2	PMC_TDO	PMC chain TDO
3	PMC_TDI	PMC chain TDI
4	PMC_TRST#	PMC chain TRST#
5		<key>
6	PMC_TMS	PMC chain TMS
7	ground	power ground
8	PMC_TCK	PMC chain TCK

5.9 JP10 – MPC8265 JTAG Header Pinout

JP10 is provided for connecting an emulator to the MPC8265 JTAG/COP interface. Emulators such as WindRiver's VisionICE II connect directly to this interface without adapters. JP10 is a dual row 16 pin header with the following pinout:



5.10 JP11 – MPC185 JTAG Header Pinout

The JP11 header allows access to the MPC185 JTAG signals. The following table defines the pinout for this dual row 10 pin connector.

Pin	Name	Functional Description
1	TMS	MPC185 JTAG TMS
2	TRST#	MPC185 JTAG RESET#
3	GND	Ground
4	TCK	MPC185 JTAG Clock
5	GND	Ground
6	NC	No Connection
7	PWRESET#	Power On Reset#
8	TDI	MPC185 JTAG Data IN
9	NC	No Connection
10	TDO	MPC185 JTAG Data OUT

5.11 JP13 – MPC180 JTAG Header Pinout

JP13 Allows access to the MPC180 JTAG pins. The pinout for JP13 is shown here.

Pin	Name	Functional Description
1	TMS	MPC180 JTAG TMS
2	TRST#	MPC180 JTAG RESET#
3	GND	Ground
4	TCK	MPC180 JTAG Clock
5	GND	Ground
6	NC	No Connection
7	PWRESET#	Power On Reset#
8	TDI	MPC180 JTAG Data IN
9	NC	No Connection
10	TDO	MPC180 JTAG Data OUT

5.12 JP15 – Power On/Off Header Pinout

The following table shows the pinout of the Power On/Off header (JP15). JP15 is intended to be used for an external power switch, such as on an ATX system chassis.

Pin	Name	Functional Description
1	toggle power	rising edge toggles power to opposite state
2	ground	power ground

5.13 JP16 – Power On Override Header Pinout

J16 is provided to bypass the power control logic on the ZPC.1900. A jumper may be placed on JP16 to continuously assert the PS_ON signal to the ATX Power Supply connector.

Pin	Name	Functional Description
1	PS_ON#	Power Supply ON control signal
2	GND	Ground

Note: PS_ON# is pulled up in the ATX power supply.

5.14 P1, P2, P3 – User IO Port Pinouts

Connectors P1 through P3 provide support signals necessary for developers that may use the ZPC.1900 platform for hardware prototyping. These connectors are 3 row x 32 (96 pin) female DIN connectors. The following tables list the pin out for the User IO connectors.

User IO Connector P1

Row A Pin Number	Signal	Row B Pin Number	Signal	Row C Pin Number	Signal
1	ATMTXEN#	1	3.3V	1	CPM_PC31
2	ATMITCA	2	3.3V	2	CPM_PC30
3	ATMTSOC	3	3.3V	3	CPM_PC29
4	ATMRXEN#	4	3.3V	4	CPM_PC28
5	ATMRSOC	5	NC	5	CPM_PC27
6	ATMRCA	6	NC	6	CPM_PC26
7	ATMTXD0	7	GND	7	CPM_PC25
8	ATMTXD1	8	GND	8	CPM_PC24
9	ATMTXD2	9	GND	9	EN_RXCLK
10	ATMTXD3	10	GND	10	EN_TXCLK
11	ATMTXD4	11	GND	11	ATMTFCLK
12	ATMTXD5	12	GND	12	ATMRFCLK
13	ATMTXD6	13	GND	13	FETHRXCK
14	ATMTXD7	14	GND	14	FETHTXCK
15	ATMRXD7	15	GND	15	CPM_PC17
16	ATMRXD6	16	GND	16	CPM_PC16
17	ATMRXD5	17	GND	17	CPM_PC15
18	ATMRXD4	18	GND	18	CD#
19	ATMRXD3	19	GND	19	CPM_PC13
20	ATMRXD2	20	GND	20	CPM_PC12
21	ATMRXD1	21	GND	21	CPM_PC11
22	ATMRXD0	22	GND	22	FETHMDC
23	SMTXD2	23	GND	23	FETHMOD
24	SMRXD2	24	GND	24	CPM_PC8
25	CPM_PA7	25	GND	25	CPM_PC7
26	CPM_PA6	26	GND	26	CPM_PC6
27	CPM_PA5	27	GND	27	CPM_PC5
28	CPM_PA4	28	GND	28	CPM_PC4
29	CPM_PA3	29	GND	29	CPM_PC3
30	CPM_PA2	30	GND	30	CPM_PC2
31	CPM_PA1	31	GND	31	CPM_PC1
32	CPM_PA0	32	GND	32	CPM_PC0

User IO Connector P2

Row A Pin Number	Signal	Row B Pin Number	Signal	Row C Pin Number	Signal
1	FETHXER	1	3.3V	1	EN_RXD
2	FETHRXDV	2	3.3V	2	EN_TXD
3	FETHTXEN	3	3.3V	3	EN_TENA
4	FETHRXER	4	3.3V	4	CPM_PD28
5	FETHCOL	5	NC	5	CPM_PD27
6	FETHCRS	6	NC	6	CPM_PD26
7	FETHTXD3	7	GND	7	CPM_PD25
8	FETHTXD2	8	GND	8	CPM_PD24
9	FETHTXD1	9	GND	9	CPM_PD23
10	FETHTXD0	10	GND	10	CPM_PD22
11	FETHRXD0	11	GND	11	CPM_PD21
12	FETHRXD1	12	GND	12	CPM_PD20
13	FETHRXD2	13	GND	13	CPM_PD19
14	FETHRXD3	14	GND	14	CPM_PD18
15	CPM_PB17	15	GND	15	ATMRXPRTY
16	CPM_PB16	16	GND	16	ATMTXPRTY
17	CPM_PB15	17	GND	17	SDCFGDT
18	CPM_PB14	18	GND	18	SDCFGCK
19	CPM_PB13	19	GND	19	CPM_PD13
20	CPM_PB12	20	GND	20	CPM_PD12
21	CPM_PB11	21	GND	21	CPM_PD11
22	CPM_PB10	22	GND	22	CPM_PD10
23	CPM_PB9	23	GND	23	CPM_PD9
24	CPM_PB8	24	GND	24	CPM_PD8
25	CPM_PB7	25	GND	25	CPM_PD7
26	CPM_PB6	26	GND	26	CPM_PD6
27	CPM_PB5	27	GND	27	CPM_PD5
28	CPM_PB4	28	GND	28	CPM_PD4
29	NC	29	GND	29	NC
30	NC	30	GND	30	NC
31	NC	31	GND	31	NC
32	NC	32	GND	32	NC

User IO Connector P3

Row A Pin Number	Signal	Row B Pin Number	Signal	Row C Pin Number	Signal
1	BR#	1	3.3V	1	3.3V
2	BG#	2	3.3V	2	3.3V
3	ABB#	3	3.3V	3	3.3V
4	DBG#	4	3.3V	4	3.3V
5	DBB#	5	3.3V	5	3.3V
6	CPUBR#	6	3.3V	6	3.3V
7	CPUBG#	7	3.3V	7	NC
8	CPUDBG#	8	NC	8	NC
9	AACK#	9	NC	9	NC
10	ARTRY#	10	NC	10	NC
11	TA#	11	NC	11	LOGIC1
12	PSDVAL#	12	NC	12	LOGIC2
13	TEA#	13	NC	13	NC
14	RSRV	14	GND	14	NC
15	TS#	15	GND	15	NC
16	NC	16	GND	16	NC
17	INT_OUT#	17	IRQ0#	17	NC
18	NC	18	IRQ1#	18	NC
19	NC	19	IRQ2#	19	NC
20	NC	20	IRQ3#	20	3.3V
21	NC	21	IRQ4#	21	3.3V
22	SPARE4	22	IRQ5#	22	3.3V
23	NC	23	IRQ6#	23	3.3V
24	SPARE6	24	IRQ7#	24	3.3V
25	NC	25	NC	25	3.3V
26	NC	26	NC	26	3.3V
27	NC	27	NC	27	NC
28	NC	28	NC	28	NC
29	MODCK1	29	NC	29	NC
30	MODCK2	30	NC	30	GND
31	MODCK3	31	NC	31	GND
32	NC	32	3.3V	32	GND

5.15 P4, P5 – TCOM Port Pinouts

Connectors P4 and P5 provide a port for a future add in board.

5.16 P6A, P6B – Ethernet Port Pinouts

The dual RJ-45 connector at P6 provides 2 standard ethernet connections. P6A is a 10/100 fast ethernet port. P6B is 10BASET only.

5.17 P7A, P7B – Serial Communication Port Pinouts

The following table shows the pinout of the DB-9M COM1 connector (P7A).

Pin	Name	Functional Description
1	-	<nc>
2	COM1_RXD	RS232 data in
3	COM1_TXD	RS232 data out
4	-	<nc>
5	ground	power ground
6	-	<nc>
7	-	<nc>
8	-	<nc>
9	-	<nc>

The following table shows the pinout of the DB-9M COM2 connector (P7B).

Pin	Name	Functional Description
1	-	<nc>
2	COM2_RXD	RS232 data in
3	COM2_TXD	RS232 data out
4	-	<nc>
5	ground	power ground
6	-	<nc>
7	-	<nc>
8	-	<nc>
9	-	<nc>

5.18 P9 – ATX Power Supply Connector Pinout

The following table shows the pinout of the ATX Power connector (P9).

Pin	Name	Functional Description
1	+3.3V	+3.3V power input
2	+3.3V	+3.3V power input
3	com	power ground
4	+5V	+5V power input
5	com	power ground
6	+5V	+5V power input
7	com	power ground
8	PWR_OK	power OK (ATX PS output), active high
9	5VSB	+5V standby
10	+12V	+12V power input
11	+3.3V	+3.3V power input
12	-12V	-12V power input
13	com	power ground
14	PS_ON	power supply turn on (ATX PS input), active low
15	com	power ground
16	com	power ground
17	com	power ground
18	-5V	not used
19	+5V	+5V power input
20	+5V	+5V power input

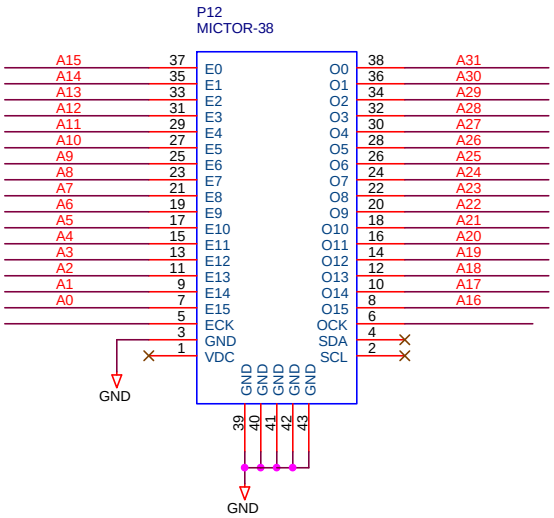
5.19 P10, P11 – PMC Card Connector Pinouts

The PMC connectors follow the standard IEEE P1386.1 pin assignments. The following table shows the ZPC.1900 PMC connector pin assignments. Please refer to the IEEE-1386 and VITA32-199x standards for further information.

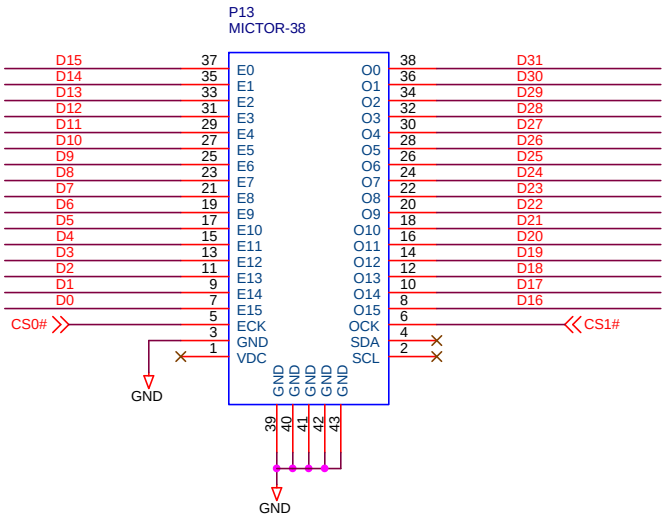
5.20 P12 through P20 – Logic Analyzer Connector Pinouts

The following sections show the pinouts of the 38-pin Mictor Logic Analyzer connectors (P12 – P20). Note that pins 39 – 43 are in the connector body and are grounded to power ground on the ZPC.1900.

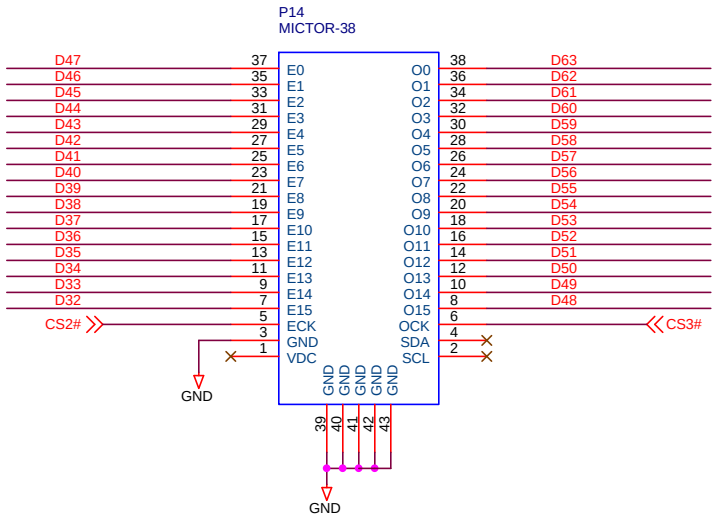
5.20.1 Connector P12 – 60x Bus Address



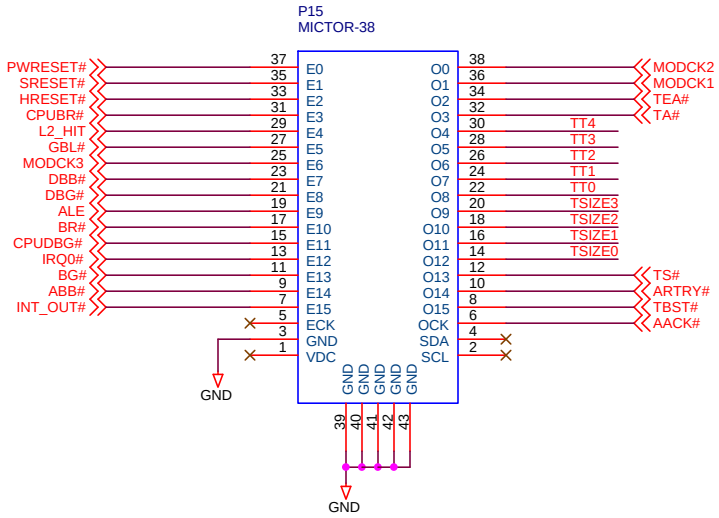
5.20.2 Connector P13 – 60x Bus Data (High)



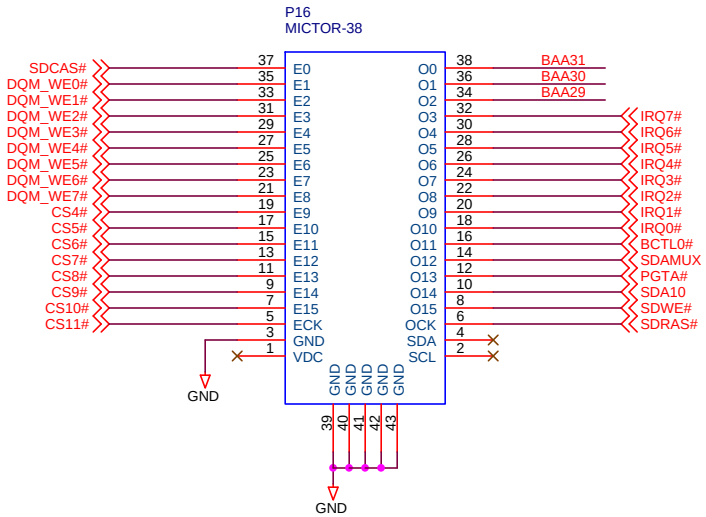
5.20.3 Connector P14 – 60x Bus Data (Low)



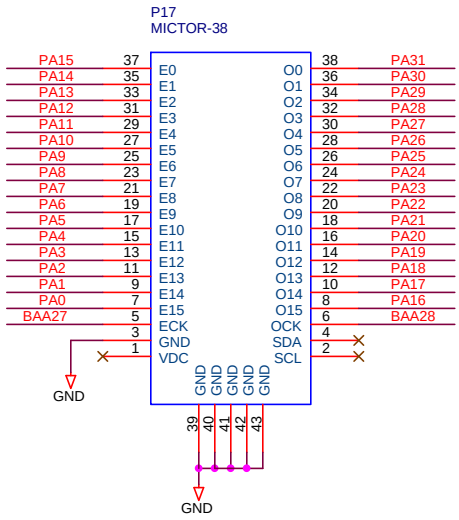
5.20.4 Connector P15 – 60x Bus Control



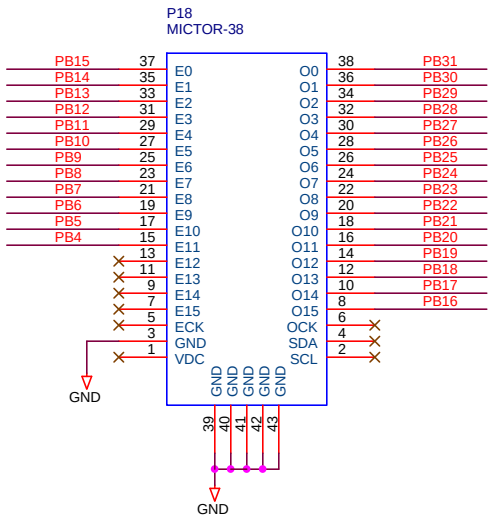
5.20.5 Connector P16 – 60x Bus Memory Control and IRQs



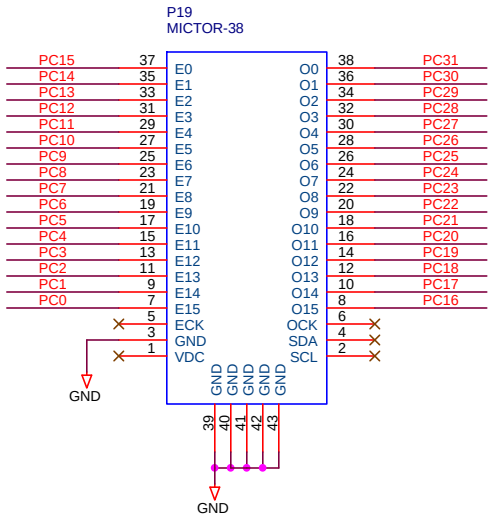
5.20.6 Connector P17 – MPC8265 Port A



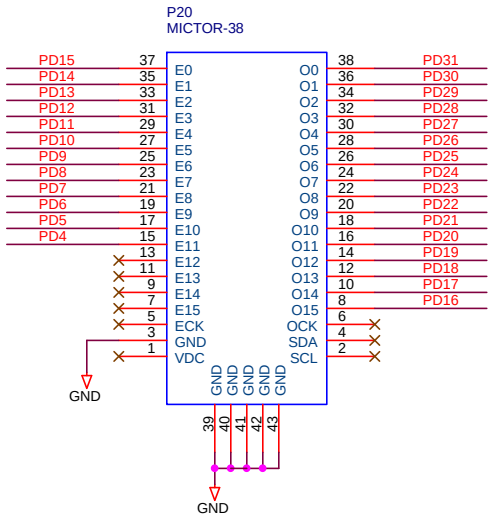
5.20.7 Connector P18 – MPC8265 Port B



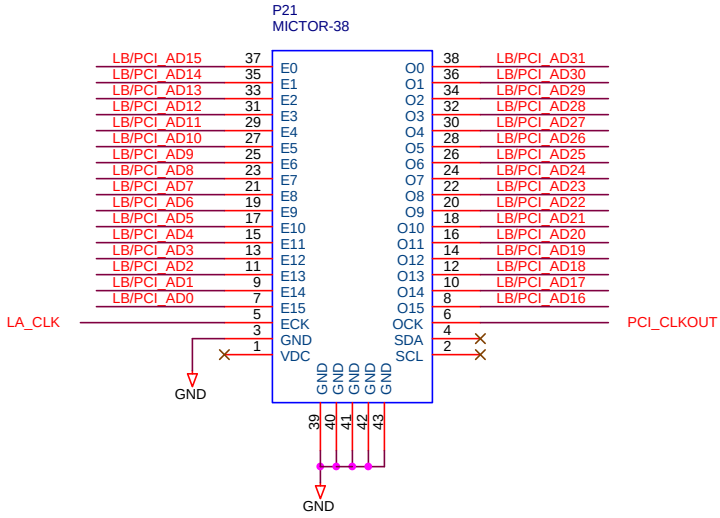
5.20.8 Connector P19 – MPC8265 Port C



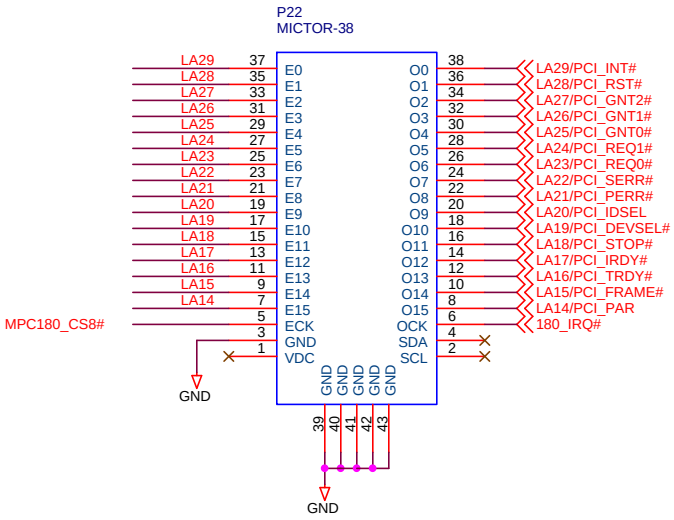
5.20.9 Connector P20 – MPC8265 Port D



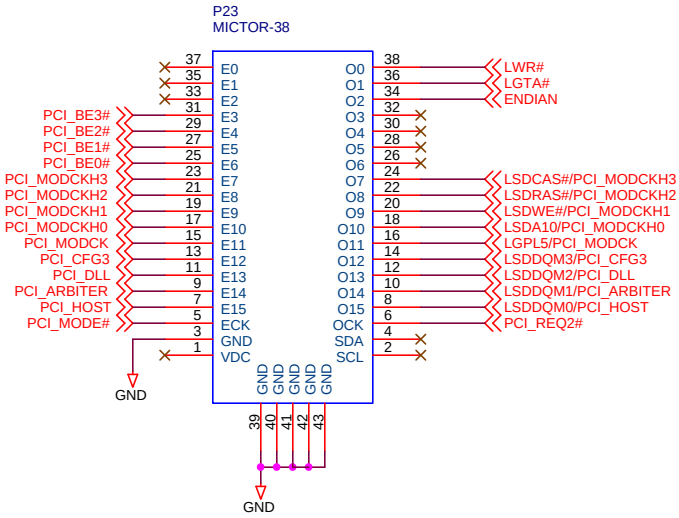
5.20.10 Connector P21 – Local Bus Data - PCI Bus Address/Data



5.20.11 Connector P22 – Local Bus Address – PCI Bus Control



5.20.12 Connector P23 – Local Bus / PCI Bus Control



6. System Initialization Programming

While the default system initialization provided by the supplied boot rom code will be sufficient for most users, some users may desire to write their own bootrom software or provide alternate initializations. To aid these users this section presents the default initialization values.

6.1 Hard Reset Configuration Word

The Hard Reset Configuration Word is programmed into FLASH memory at locations 0, 8, 10, and 18.

Contents at FLASH Address				Results in this configuration	
0x0	**0x8**	**0x10**	**0x18**	Bus Mode	Description
14	82	02	05	Local Bus	8 bit Boot Port for on board FLASH
1C	82	02	05	Local Bus	32 bit Boot Port for FLASH SIMM module
14	82	06	05	PCI Bus	8 bit Boot Port for on board FLASH
1C	82	06	05	PCI Bus	8 bit Boot Port for FLASH SIMM module

Note: TBD values to be used for Linux bootrom.

The values from the above table set the following parameters:

- Internal arbitration
- Internal memory controller
- Core enabled
- 60x Bus Mode (multi-master)
- Boot Port size (either 8 or 32 bit flash)
- Exception vectors at 0xfff0_0000
- Internal space appears as 64 resource to other masters
- Initial value for SIUMCR[L2CPC] = b10, L2 Cache pins are used for BADDR29:31
- Data Parity pin option set to use IRQs
- Internal space (IMMR) base address = 0x0F00_0000
- Boot memory space = 0xFE00_0000
- Bus Busy enabled
- Master Requests are not masked
- Local bus pin configuration = Local Bus or PCI Bus
- Address parity pin configuration = BNKSEL
- CS10PC = CS10
- MODCK_H = 0x5 for Local Bus frequency configuration

6.2 MPC8265 System Control Register Programming

IMMR	0x0F000000
SIUMCR	0x42200000 Local bus mode
	0x42600000 PCI bus mode
SYPCCR	0xFFFFFFC3
BCR	0x90400000
PSDMR	0x414EB45A
PPC_ACR	0x03
PPC_ALRH	0x30126745
SCCR	0x0000001 Local Bus Mode
	0x0000119 PCI Bus Mode

6.3 Memory Controller Register Programming

Register	Device	Bus	Value	Description
BR0	On Board 2MB Flash	60x	FE000801	8 bit
	*option – Flash SIMM module**		FE001801	*32 bit*
OR0	On Board 2MB Flash		FE000856	
	*option – Flash SIMM module**		FE000860	
BR1	16 MB FLASH SIMM Bank 2	60x	FC001801	32 bit Reserved for future use
OR1			FF000870	
BR2	SDRAM	60x	00000041	64 bit, 4 banks
OR2			FC0028C0	
BR3	SDRAM	60x	00000000	Not used for 64MB
OR3			00000000	
BR4	8 MB LB SDRAM	Local	04001861	
OR4			FF803480	
BR5	8 KB EEPROM	Local	22000801	8 bit
OR5			FFFF03F6	
BR6	FLASH SIMM	60x	E0001801	32 bit
	*option - On Board 2MB Flash**		E0000801	8 bit
OR6	FLASH SIMM		FF000860	
	*option - On Board 2MB Flash**		FE000856	
BR7	User Logic	Local	21000801	On board resources: switches, LEDs, registers
OR7			FFFF03F6	
BR8	MPC180	Local	05001881	
OR8			FFC00000	
BR9	TCOM Slot	Local	TBD	
OR9			TBD	
BR10	Not Used			
OR10				
BR11	Not Used			
OR11				

* option – use when board is configured to boot from Flash SIMM module.

6.4 Chip Select, IDSEL and Interrupt Mapping

The following table shows the default chip select and interrupt connections on the ZPC.1900 platform

Device	Chip Select	Interrupt	Recommended Address
64MB SDRAM	CS2		00000000 – 03FFFFFF
SDRAM reserved	CS3		reserved for future expansion
MPC185	none – 60x bus	1	30000000 -
Local Bus SDRAM	CS4**		04000000 – 047FFFFF**
MPC180	CS8**	2	05000000 – 05FFFFFF**
User Logic	CS7		21000000 – 2100FFFF
8KB EEPROM	CS5		22000000 – 2200FFFF
16MB SIMM Flash	CS6		E0000000 – E0FFFFFF
Flash SIMM reserved	CS1		reserved for future expansion
2MB on-board Flash	CS0		FE000000 – FFFFFFFF
PMC Slot	none	5*	60000000 – 6FFFFFFF
TCOM Slot	CS9	6, 7	
User IO Ports		0	
Fast Ethernet		3	
MPC8265 PCI IRQ		5	

****Not available in PCI mode**

***On Revision C boards, the PMC IRQ will move to IRQ4.**

6.5 PCI IDSEL

The PMC card slot connects to IDSEL AD16.
The MPC8265 PCI agent connects to IDSEL AD17.

7. Local Register Definitions

Function	R/W	Size	Address
Flash Presence Detect	R	Byte	21000000
User Switches	R	Byte	21000001
Board Revision	R	Byte	21000002
LED Register	R/W	Byte	21000003
Mode Register	R	Byte	21000004

7.1 FLASH Presence Detect

The flash presence detect register is a read-only register that returns the value of the PD1-7 pins on the Flash SIMM Module.

FPD Register (0x2100 0000):

bit 0	1	2	3	4	5	6	bit 7
0	FPD7	FPD6	FPD5	FPD4	FPD3	FPD2	FPD1

7.2 User Switch Register

The User Switch Register returns the value set by the 8 position switch at S1. This is a read-only register.

User Switch Register (0x2100 0001):

bit 0	1	2	3	4	5	6	bit 7
S1-8	S1-7	S1-6	S1-5	S1-4	S1-3	S1-2	S1-1

7.3 Board Revision Register

The Board Revision Register returns a value programmed in the User Logic PLD that is set to the current revision level of the board. Revision B PCBs will return the value 0x02. This register is read-only.

Board Revision Register (0x2100 0002):

bit 0	**1**	**2**	**3**	**4**	**5**	**6**	**bit 7**
Rev.	Rev.	Rev.	Rev.	Rev.	Rev.	Rev.	Rev.

7.4 LED Register

The LED register is an 8 bit read/write register allowing user's to illuminate 8 LEDs provided on the ZPC.1900 board edge.

Board Revision Register (0x2100 0003):

bit 0	**1**	**2**	**3**	**4**	**5**	**6**	**bit 7**
LED 0	LED 1	LED 2	LED 3	LED 4	LED 5	LED 6	LED 7

7.5 Mode Register

The mode register returns the state of the PCI/Local Bus select jumper JP9. The Mode Register is read-only.

Mode Register (0x2100 0003):

bit 0	1	2	3	4	5	6	bit 7
X	X	X	X	X	X	X	B_MOD

X: Unused, don't care (R)

B_MOD: Bus Mode (R)
1 = PCI bus Mode
0 = Local Bus Mode

8. Optional Configurations

The ZPC.1900 provides a flexible platform for both software and hardware developers. Most of the functions on the board can be disconnected by de-soldering the appropriate configuration resistors, allowing a developer to prototype alternate implementations or even new functions onto the platform. Zephyr Engineering also provides design services to other companies to help reduce the time to market for products similar to this one.

8.1 Peripheral Isolation

For debugging, each of the following peripherals may be isolated by removing configuration resistors.

To Isolate:	**Remove:**
User IO ports	RN62-RN77
Fast Ethernet	RN38-RN40
10 Base-T	RN42-RN43
RS232	RN45
TCOM SLOT	RN11-RN22, RN28

8.2 PCI Configuration Resistors

Resistors R47 through R55 set build configuration options for the PCI bus.
The following resistors should be populated for the default configuration: R48, R49, R50, R51, R53, R54.
The following resistors are not populated for the default configuration: R47, R52, R55.

9. Warranty and Support Information

9.1 Warranty

All Zephyr Engineering Products include a 1 year limited warranty.

9.2 Support

The ZPC.1900 platform is supported at no additional charge for a period of 60 days following the date of shipment. Please contact Zephyr Engineering, Inc. for extended support agreements. Technical support personnel may be reached by email at support@zpci.com. Our technical support hours are Monday – Friday 8:30 A.M. to 5:00 P.M. Mountain Standard Time.

Additional information for the ZPC.1900 may be found on our web page at www.zpci.com.