Zephyr Engineering, Inc

User's Manual, ZPCI.2900, Rev B

Rev 1.0

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1. Introduction

The ZPCI.2900 is an ATX form-factor quad PMC carrier board. One slot is a Monarch CPU type, and the other three are standard PMC slots. All slots are 64-bit bus width and run at either 33 or 66 MHz.

2. Jumper Definitions

The ZPCI.2900 contains 5 jumpers, JP1 – JP5. The functions of these jumpers are described in the following table.

Jumper	Jumper Name	Default	Pins	Functional Description
JP1	Chassis Ground Option	open	open	do not connect grounds
			shorted	connect chassis ground to power ground
JP2	5V load enable	open	open	disconnect 5W load from +5V power rail
			shorted	place 5W load on +5V power rail
JP3	Force 33MHz operation	open	open	allow M66EN to follow PCI bus level
			shorted	pull M66EN low on PCI bus
JP4	Boot Flash Bank Select	2-3	2-3	Boot from Bank A (PrPMC800 FLASH)
			1-2	Boot from Bank B (ZPCI.2900 FLASH)
JP5	Power-on Override	open	open	ATX PS_ON controlled by SW1, SW2 and J9
			shorted	ATX PS_ON held low (always on)

3. Connector Definitions

The ZPCI.2900 contains 9 connectors (in addition to the PMC connectors). The function of each connector is listed in the following table.

Number	Name	Type	Functional Description
J1	Emulator	16-pin dual-row 0.1” pitch	connection for BDM emulator
J2	Debug Port	DB-9M	RS-232C debug port (slot 1)
J3	Debug Port	10-pin dual-row 0.1” pitch	in parallel with J2
J4	ATX Power	20-pin male ATX power	Power input
J5	PMC JTAG	8-pin single-row 0.1” pitch	PMC slot JTAG chain
J6	ISP download	8-pin single-row 0.1” pitch	Arbiter CPLD ISP program port
J7	Logic Analyzer	38-pin MICTOR	Logic Analyzer connection
J8	Reset	2-pin single-row 0.1” pitch	reset from external pushbutton
J9	Power Control	2-pin single-row 0.1” pitch	power on/off from external pushbutton

4. Switch Functions

There are 3 switches on the ZPCI.2900. The function of each switch is listed in the following table.

Number	Name	Type	Functional Description
SW1	Power On Override	toggle	Keep power on regardless of J9 or SW2
SW2	Power On/Off	pushbutton	toggle power on or off
SW3	Reset	pushbutton	assert power-on reset

5. LED Functions

There are 5 LEDs on the ZPCI.2900. The function of each LED is listed in the following table.

Number	Name	Functional Description
DS1	INTA	when lit, PCI bus INTA is asserted
DS2	INTB	when lit, PCI bus INTB is asserted
DS3	INTC	when lit, PCI bus INTC is asserted
DS4	INTD	when lit, PCI bus INTD is asserted
DS5	Power	when lit, ATX +5V in on

6. Connector Pinouts

6.1 PMC Connectors

The PMC connectors follow the standard Monarch pin assignments. The following table shows the ZPCI.2900 connector numbers assigned to each slot. Please refer to the IEEE-1386 and VITA32-199x standards for the PMC pinouts.

	Slot 1 Monarch	Slot 2 non-Monarch	Slot 3 non-Monarch	Slot 4 non-Monarch
IEEE Designator				
PMC J11	J11	J21	J31	J41
PMC J12	J12	J22	J32	J42
PMC J13	J13	J23	J33	J43
PMC J14	J14	none	none	none

6.2 Emulator Connector (J1) Pinout

The following table shows the pinout of the Emulator connector (J1).

Pin	Name	Functional Description
1	CPUTDO	PrPMC800 J14-6: CPUTDO
2	-	<nc>
3	CPUTDI	PrPMC800 J14-5: CPUTDI
4	CPUTRST_L	PrPMC800 J14-7: CPUTRST_L
5	-	<nc>
6	+3.3V	+3.3V power
7	CPUTCK	PrPMC800 J14-11: CPUTCK
8	-	<nc>
9	CPUTMS	PrPMC800 J14-12: CPUTMS
10	-	<nc>
11	SRESET_L	PrPMC800 J14-13: SRESETL
12	-	<nc>
13	CPURST_L	PrPMC800 J14-14: CPURST_L
14	-	<nc>
15	CKSTPO_L	PrPMC800 J14-15: CHKSTOPO
16	ground	power ground

6.3 Debug Port Connector (J2) Pinout

The following table shows the pinout of the DB-9M Debug Port connector (J2).

Pin	Name	Functional Description
1	-	<nc>
2	RXD	PrPMC800 J14-4: RXD
3	TXD	PrPMC800 J14-3: TXD
4	-	<nc>
5	ground	power ground
6	-	<nc>
7	-	<nc>
8	-	<nc>
9	-	<nc>

6.4 Debug Port Connector (J3) Pinout

The following table shows the pinout of the 10-pin header Debug Port connector (J3).

Pin	Name	Functional Description
1	-	<nc>
2	-	<nc>
3	RXD	PrPMC800 J14-4: RXD
4	-	<nc>
5	TXD	PrPMC800 J14-3: TXD
6	-	<nc>
7	-	<nc>
8	-	<nc>
9	ground	power ground
10	-	<nc>

6.5 ATX Power Connector (J4) Pinout

The following table shows the pinout of the ATX Power connector (J4).

Pin	Name	Functional Description
1	+3.3V	+3.3V power input
2	+3.3V	+3.3V power input
3	com	power ground
4	+5V	+5V power input
5	com	power ground
6	+5V	+5V power input
7	com	power ground
8	PWR OK	power OK (ATX PS output), active high
9	5VSB	+5V standby
10	+12V	+12V power input
11	+3.3V	+3.3V power input
12	-12V	-12V power input
13	com	power ground
14	PS_ON	power supply turn on (ATX PS input), active low
15	com	power ground
16	com	power ground
17	com	power ground
18	-5V	-5V power input
19	+5V	+5V power input
20	+5V	+5V power input

6.6 PMC JTAG Connector (J5) Pinout

The following table shows the pinout of the PMC JTAG connector (J5).

Pin	Name	Functional Description
1	+3.3V	+3.3V power
2	J42 TDO	PMC chain TDO
3	J12 TDI	PMC chain TDI
4	TRST#	PMC chain TRST#
5		<key>
6	TMS	PMC chain TMS
7	ground	power ground
8	TCK	PMC chain TCK

6.7 ISP Download Connector (J6) Pinout

The following table shows the pinout of the ISP Download connector (J6).

Pin	Name	Functional Description
1	+3.3V	+3.3V power
2	ARB_TDO	CPLD TDO
3	ARB_TDI	CPLD TDI
4	ispEN#	CPLD BSCAN# input
5		<key>
6	ARB_TMS	CPLD TMS
7	ground	power ground
8	ARB_TCK	CPLD TCK

6.8 Logic Analyzer Connector (J7) Pinout

The following table shows the pinout of the38-pin Mictor Logic Analyzer connector (J7). Note that pins 39 – 43 are in the connector body and are grounded to power ground on the ZPCI.2900.

Pin	Name	Functional Description
1	-	<nc>
2	-	<nc>
3	ground	power ground
4	-	<nc>
5	CLK_LA1	system clock (33 or 66 MHz)
6	-	<nc>
7	-	<nc>
8	GNT8#	arbiter GNT8#
9	-	<nc>
10	GNT7#	arbiter GNT7#
11	-	<nc>
12	GNT6#	arbiter GNT6#
13	-	<nc>
14	GNT5#	arbiter GNT5#
15	-	<nc>
16	GNT4#	arbiter GNT4#
17	-	<nc>
18	GNT3#	arbiter GNT3#
19	-	<nc>
20	GNT2#	arbiter GNT2#
21	-	<nc>
22	GNT1#	arbiter GNT1#
23	TCK	TCK to J11-1/J21-1/J31-1/J41-1
24	REQ8#	arbiter REQ8#
25	TRST#	TRST# to J12-2/J22-2/J32-2/J42-2
26	REQ7#	arbiter REQ7#
27	TMS	TMS to J12-3/J22-3/J32-3/J42-3
28	REQ6#	arbiter REQ6#
29	J12_TDI	TDI to J12-5
30	REQ5#	arbiter REQ5#
31	J12_TDO	TDO from J12-4/J22-5
32	REQ4#	arbiter REQ4#
33	J22_TDO	TDO from J22-4/J32-5
34	REQ3#	arbiter REQ3#
35	J32_TDO	TDO from J32-4/J42-5
36	REQ2#	arbiter REQ2#
37	J42_TDO	TDO from J42-4
38	REQ1#	arbiter REQ1#

6.9 Reset Connector (J8) Pinout

The following table shows the pinout of the Reset connector (J8).

Pin	Name	Functional Description
1	reset	low causes reset assertion; logic holds low for 500 ms
2	ground	power ground

6.10 Power Control Connector (J9) Pinout

The following table shows the pinout of the Power Control connector (J9).

Pin	Name	Functional Description
1	toggle power	rising edge toggles power to opposite state
2	ground	power ground

7. Interrupt and IDSEL Routing

The following table shows the INTx, IDSEL, REQx/GNTx, REQBx/GNTBx and JTAG connections for each PMC slot.

	Slot 1 J11/J12/J13/J14	Slot 2 J21/J22/J23	Slot 3 J31/J32/J33	Slot 4 J41/J42/J43
Interrupt	INTA#	INTB#	INTC#	INTD#
IDSEL	AD11	AD12	AD13	AD14
IDSELB	AD15	AD16	AD17	AD18
REQ	REQ1#	REQ2#	REQ3#	REQ3#
GNT	GNT1#	GNT2#	GNT3#	GNT4#
REQB	REQ5#	REQ6#	REQ7#	REQ8#
GNTB	GNT5#	GNT6#	GNT7#	GNT8#
TDO	J12-TDO	J22-TDO	J32-TDO	J5-2 (chain TDO)
TDI	J5-3 (chain TDI)	J12-TDO	J22-TDO	J32-TDO

8. PrPMC800 support

The ZPCI.2900 supports the PrPMC800 BDM emulator port, RS232C debug port and Bank B boot FLASH. The ZPCI.2900 does not support the PrPMC800 on-board Ethernet port.

8.1 Emulator Port

The PrPMC800 BDM emulator port is connected to J1, a 16-pin (dual row) right-angle 0.1” pitch connector located in the ATX I/O area.

8.2 Debug Port

The PrPMC800 serial debug port is connected to J2, a DB-9M connector located in the ATX I/O area. It is also connected to J3, a 10-pin (dual row) connector suitable for use with IDC ribbon cable connectors. There is only one debug port; use either J2 or J3 to connect to it.

8.3 Boot Flash

The PrPMC800 has connections for an external bank of boot FLASH. The ZPCI.2900 provides this external bank. Header JP4 allows booting from either the PrPMC800 FLASH (JP4-2 shorted to JP4-3) or the ZPCI.2900 FLASH (JP4-1 shorted to JP4-2). The ZPCI.2900 FLASH is comprised of two Am29LV040B-120JC parts, each of which is 512K x 8 bits, for a total bank size of 1M byte.

9. Special Features

9.1 Frequency Auto-detect

The ZPCI.2900 supports the M66EN signal on PMC connectors J12/J22/J32/J42. Any PMC card can pull this low to force 33 MHz operation. Installing a jumper on JP3 also forces 33 Mhz

operation, simply by pulling down M66EN on the bus. The ZPCI.2900 monitors the M66EN line and sends the appropriate clock (33 or 66 MHz) to all of the PMC cards.

9.2 PCI Bus Arbiter

The ZPCI.2900 bus arbiter is a round-robin fairness type, with park on last master. It is implemented in an in-circuit-programmable CPLD.

9.3 Power Control

The power control is designed to be as flexible as possible, allowing the ZPCI.2900 to be used either stand-alone on the lab bench or as part of a system in a standard ATX-style case. In the case of an ATX system, J8 can connect directly to the reset button on the case. In a like manner, the J9 connector can connect to the momentary power on/off pushbutton on the case. For local use, SW2 connects in parallel with J9 for power on/off. Similarly, SW3 is on parallel with J8 for local reset. In the case when no power switching is desired and the unit must stay on, SW1 overrides J9 and SW2 to keep power always on.